UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

January 1 - January 31, 1956

I. MATHEMATICAL RESEARCH AND PROGRAMMING. (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Boolean Algebra and Switching Circuits

Progress in the study of speed-independent circuits has been made through the expression of the condition for speed independence in algebraic form. This should make it possible to provide a more algebraic approach to the problem of synthesizing such circuits. An earlier condition, which was sufficient, led to totally sequential circuits rather than the larger class of speed-independent circuits.

A preliminary version of a report on examples of speed-independent circuits has been completed, and emphasis will now be shifted to speed-independent information-handling systems and the study of speed-independent adders.

Floating Address Routine

The parts of the floating address program which treat interludes have been written and will remain during use of the routine in the Williams memory in locations from 999 to 1019. These parts will contain a) words which cause transfer of memory contents in locations 0 to 998 to the magnetic drum whenever an interlude ends and more reading is to be done; b) a bootstrap to extract the floating address routine from the drum and place it in the Williams memory; c) a section which calls for the program from the drum, puts it into the Williams memory, and transfers control to the word specified by the last N termination; d) information in a single word to record whether the reading is being done for the first time or after an interlude (with directive data being stored if necessary); e) a word which contains information about the length of the address list.

The Decimal Order Input has been rewritten so as to be placed beginning at location 200 and has been modified so that N terminations are not immediately obeyed but merely initiate the setting of true addresses in the program and so that N terminations which transfer control to the Decimal Order Input are immediately obeyed (since they are orders initiating further reading in from the tape).

Continued Fraction Expansions

Further study has been made of the use of continued fraction expansions and a general technique for developing power series representations of functions into continued fractions has been programmed.

Sturm-Liouville Systems

Three more subroutines for the Sturm-Liouville problem were written. This completes the subroutine requirements for the first experiment to be tried. The most important phase of the first experiment is to determine whether using higher order approximations to the function actually leads to greater accuracy.

Code Checking Routines

Most of the features of the combined post mortem routine which will be placed on the magnetic drum have been checked using the fast memory. The final and complete code check, using the drum, should reveal only minor discrepancies, if any.

II. ANALYTICAL PROGRAM. (This work is supported in part by the National Science Foundation under Grant G-1221.)

Work continues on general solutions of the Einstein gravitational field equations for a plane-symmetric space-time when the gravitational field is due to the presence of a perfect fluid described by an arbitrary caloric equation of state. An approximate procedure has been devised for dealing with these equations. This involves using as the zeroth order approximation to the solution of a general relativity problem the solution of a corresponding problem in special relativity in orthogonal Lagrangian coordinates. The theory of hydrodynamics in the special theory of relativity has been formulated in terms of such coordinates and methods of solving the resulting equations in terms of characteristic variables have been devised.

III. PROGRAM LIBRARY.

In January the following two new programs were added to the active program library.

Y-2 (200) — Drum Playback for Routines. 46 words. This is an open routine which extends the use of the Decimal Order Input. It will read from an input tape just as the Decimal Order Input (Library Routine X-1) does, or it will play back to the Williams memory routines which have been placed on the magnetic drum by recording routine Y-3. Reading from the tape stops and drum playback begins when a directive on the tape is read; tape reading is resumed when a terminating symbol place with the routine on the drum by Y-3 is read.

P-3 (204) — Combined Integer Print. 35 words. This is a closed routine with one program parameter. It provides more flexibility than other integer print routines, both zero suppression and space suppression being available. It will not hang up if the number of digits specified to be printed is less than the number in the integer, and it will correctly print to 12 decimal places the quantities $2^{39} - 1$ and -2^{-39}, which are respectively the greatest positive and greatest negative integer capable of being stored in one location.

The following program was added to the auxiliary program library.

N-10 (205) — Input a Sequence of Integers with Sum Check. 36 words. This routine is intended primarily for

long data tapes which are used repetitively. A sum check constant at the end of the tape is compared with a sum accumulated during input.

IV. MACHINE USE.

During January specifications were presented for 18 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 723. Numbers followed by T are for theses.

723 Computer. Sturm-Liouville Systems. This program is for the investigation of numerical solutions of Sturm-Liouville differential equations.

724 Structural Research. Deflection of a Non-Linear System with Variable Coefficients. This problem uses the same program as that used with Problem 630.

725 Psychology. Oblimax Rotation of Factor Vectors. The purpose of this routine is similar to that of the Quartimax program. It transforms a set of factor vectors to a new set such that a particular function is maximized and is an analytic approach to the simple structure of L. L. Thurstone.

726 Psychology. Pattern Analysis of the Manson Personality Inventory. The research is designed to develop configural scoring keys of items from the Manson Personality Inventory which will discriminate between three groups of subjects. The keys will be established with an experimental sample. Use will be made of several programs from the Psychology Program Library.

727 Physics. V Center Spin Hamiltonian Eigenvalues. A magnetic spin resonance of a V center (a hole in a halogen ion existing at a positive ion vacancy or double vacancy) has been observed in some of the alkali halides. This problem

is concerned with the nature and degree of removal of the degeneracy of the energy levels representing the hole in the presence of a large dc magnetic field. The solution requires finding eigenvalues and eigenvectors of a 32 x 32 matrix.

728 T Physical Education. Interrelationships of Certain Anthropological Measurements, Specific Gravity and Basal Oxygen Intake. A set of 37 measurements were taken on 100 subjects and will be studied through the calculation of product-moment correlations.

729 State Water Survey. Off-Center Rain Gauging. The purpose of this problem is to determine an estimate of the error involved in sampling in an area when a gauge is located at various distances from the geographical center of the area. Data have been obtained from 12,374 observations, and a correlation and regression technique of analysis will be used.

730 Computer. Demonstrate Counting. This is a demonstration program.

731 Agricultural Economics. Storage and Movements of Cash Grain. A multiple regression analysis will be used to determine the relative importance of various supply factors on weekly cash corn prices, using variables which will indicate the effect of the level of stocks in Chicago and primary markets and the rate of movement to and from these markets.

732 Education. Judges' Rating Plans. A group of n judges is used to rate n persons. Because of the time needed to rate each person and because of the complexity of the rating situation, each judge will be asked to rate only r out of the n persons. The problem is how to assign the r persons to each judge so that the number of discriminations among persons is at a maximum and so that each person is rated an equal number of times. A systematic study will be made for some values of small r.

733 Physiology (University of Chicago). Diurnal Variations in Heart Rate, Blood Pressure and Work Output. This investigation aims at clarifying the relation between performance on sensory-motor tasks and the physiological condition of the performer. The analysis is being carried out through the use of auto-correlogram plots and power spectrum functions.

734 T Economics. Relation of Price and Other Factors to the Production of Corn in the Corn Belt. Multiple correlation procedures will be used to fit a single equation model to data for 30 to 34 years.

735 T Psychology. Comparison of Distractibility of Intellectually Normal and Mentally Defective Subjects. Pearson product moment correlations will be computed for four 11 x 11 matrices.

736 Speech. Approximations to English Based on the Transition Probability of Phonemes. The technique described by Shannon and Weaver for the analysis of English by use of conventional orthographic units will be used to study the spoken language in which the significant unit is the phoneme (the minimal distinctive sound unit of the language). Analysis will be made of a phonemized corpus of about 20,000 units in length.

737 T Theoretical and Applied Mechanics. Numerical Solution to the Extension of a Perforated Tension Strip. A thin strip containing a hole is placed in tension. The problem is to determine the components of displacement at a finite number of mesh points on the strip and to determine the resulting state of stress at each point. The solution will be carried out primarily through solving sets of 90 simultaneous linear algebraic equations, evaluating some algebraic equations, and calculating finite difference approximations to first and second partial derivatives.

738 T Institute of Communications Research. Factors Affecting Audience Evaluation of Radio Drama Content. The data analyzed in this study were obtained from three tests administered to two hundred fifteen high school students. The analysis will be carried out with Library Routine K-2.

739 Physics. Gamma Ray Cross Sections in Helium and Lithium. In evaluating the pseudodeuteron model for the photodisintegration of complex elements it is necessary to evaluate an integral involving an exponential with a fourth degree polynomial in the exponent, a Jacobian, and a bremmstrahlung spectrum. There are three parameters, and the integral must be evaluated about 3,000 times. An interlude will be used to evaluate one of the functions for 51 values of the independent variable, and Simpson's rule will be used to calculate the integral.

740 Structural Research. Natural Frequencies of a Simply Supported Beam with Distributed and Concentrated Mass. The program uses the inverse interpolation program H-1 to search for the natural frequency of a simply supported elastic beam with distributed and concentrated mass. The natural frequency is defined by means of an expression involving circular and hyperbolic sines.

Table I shows distribution of machine time for the month of January.

TABLE I

Regular Maintenance and Illiac Engineering	51:42
Unscheduled Maintenance or Repair	3:33
R.A.R.	5:45
Leapfrog	64:14
Drum Engineering	15:50
Wasted	:06

TABLE I (Cont.)

Use by Departments

Computer Group	9:54
Physics	90:46
Control Systems Laboratory	59:30
Structural Research	41:24
Structural Research (AF 24994)	2:05
Psychology	6:28
Theor. and Applied Mech. (N6ori-07135)	10:40
Electrical Engineering	:37
Electrical Engineering (AF 3220)	:40
Chemistry	34:55
Agriculture	5:13
Economics	4:04
Institute of Communications Research	1:11
MURA	59:16
Classes	20:27
Demonstrations	2:26
Miscellaneous	7:35
Total	498:21

V. ERROR FREQUENCY AND ANALYSIS.

The machine is normally used for "engineering" and maintenance between 8:00 A.M. and 12:00 N, and for a check of its performance between 6:00 and 6:30 P.M. of each weekday. Since the periods between 8:00 A.M. and noon, together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between noon and 8:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind,

a summary table has been prepared using the period between noon and 8:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 6:00-6:30 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This overall system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for January.

TABLE III

Summary of Errors

Arithmetic Unit	0
Control	0
Reading Combined with Punching	0
Reading Only	7
Punching Only	1
Memory	6
Reader Control	0
Input Output Control	0
Fuse Blew in Circuit #8	1
Scope Advancing Film without an Order from Illiac	1
Total	16

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
1/3/56	20:00	:00	0		:00	3:05	0
1/4/56	20:00	:00	0		:00	1:59	0
1/5/56	20:00	:00	0		:00	:47	0
1/6/56	20:00	:00	0		:00	1:31	0
1/9/56	20:00	:00	0		:00	2:59	0
1/10/56	20:00	:00	0		:00	1:57	0
1/11/56	19:57	:00	0		:03	1:29	0
1/12/56	20:00	:00	0		:00	1:18	0
1/13/56	20:00	:00	0		:00	:59	0
1/16/56	11:16	:59	1	(1) $0 \rightarrow 1$, 2^{-36} memory filament short 6AQ5(V4)	:00	1:57	1 *
1/17/56	11:44	:35	1	(1) Error in memory position 2^{-2}	:00	:58	0 *
1/18/56	19:25	:35	4	(1) Leapfrog - Input Output Error. Sprocket hole bad, (Reader H) (2) Reading incorrectly. (Reader I) (3) Reader H seems to be bad. (4) Reader H bad.	:00	1:11	1
1/19/56	19:44	:16	1	(1) Changed CRT in 2^{-31}.	:00	1:43	0
1/20/56	20:00	:00	0		:00	1:47	0
1/23/56	18:30	:01	1	(1) Fuse blew circuit No. 8.	:00	1:17	0
1/24/56	19:57	:03	1	(1) Reader K - 5th hole low	:00	1:00	0
1/25/56	19:37	:23	2	(1) Memory error 2^{-31} (2) Memory error 2^{-31}	:00	1:46	0
1/26/56	19:59	:01	1	(1) Scope advancing film without orders from Illiac	:00	2:12	0
1/27/56	19:56	:04	2	(1) Punch cut tape in two. (2) Reader K evidently in error.	:00	4:30	1

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
1/30/56	19:29	:31	2	(1) Memory error 2^{-9} (2) Input Output error.	:00	2:56	2
1/31/56	20:00	:00	0		:00	1:01	0
				* Computer turned off at midnight			
	399:34	3:28	16		:03	38:22	5

VI. COMMENTS ON ILLIAC DRUM MEMORY.

Trouble-shooting of the final drum storage unit continued during the month of January. It was necessary to delay the record strobe pulse in order that the initial digits could be recorded correctly. Delaying the record strobe necessitated repositioning the sensing and gating pulses used in the playback and correction circuits. It was also found that the digit recorded during the origin gap was incorrectly played back. This difficulty was cured by introduction of an "A delay" pulse which was triggered by the B pulse. The A pulse is now triggered by the A delay pulse rather than from the control track signal.

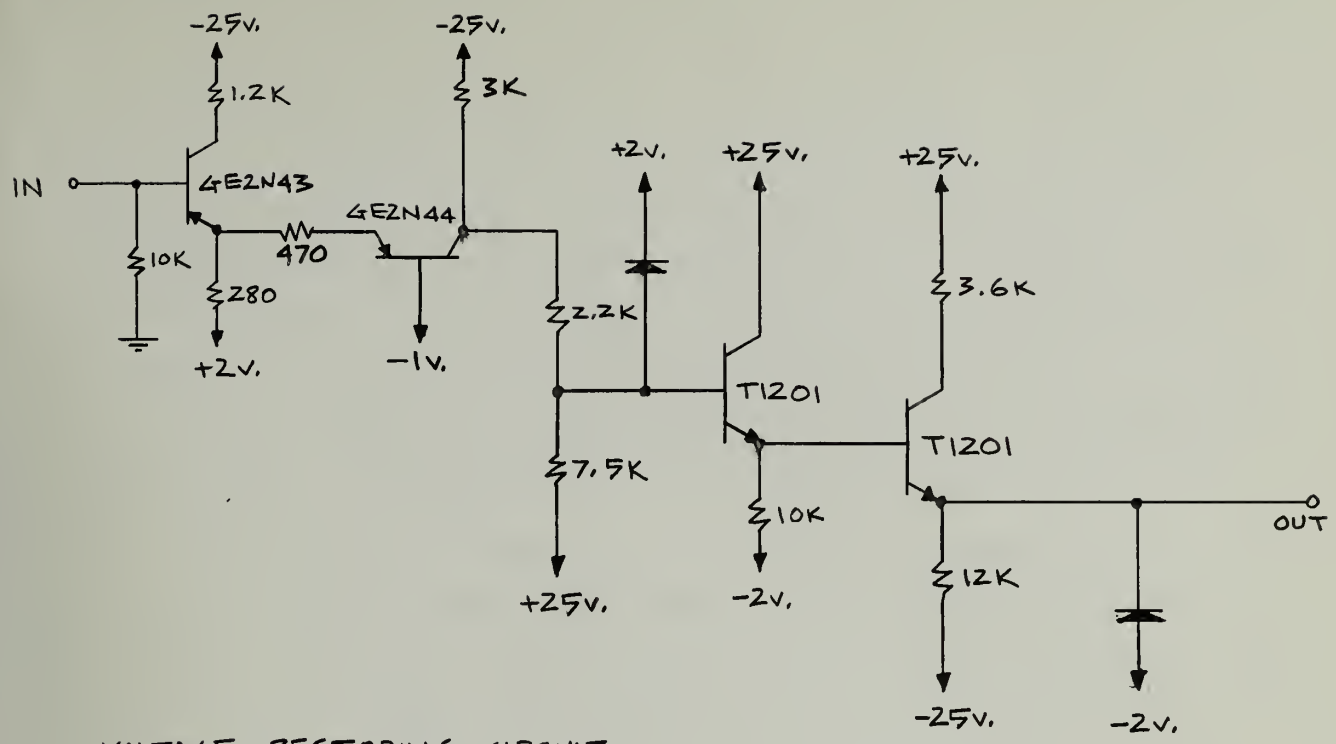
At the end of the month the drum test code was running on all 200 tracks with a failure rate of 20 to 30 failures during a 20 minute interval.

VII. RESEARCH ON COMPUTER COMPONENTS. (This work is supported in part by the Office of Naval Research under Contract N6ori-07124.)

Transistor Test Computer

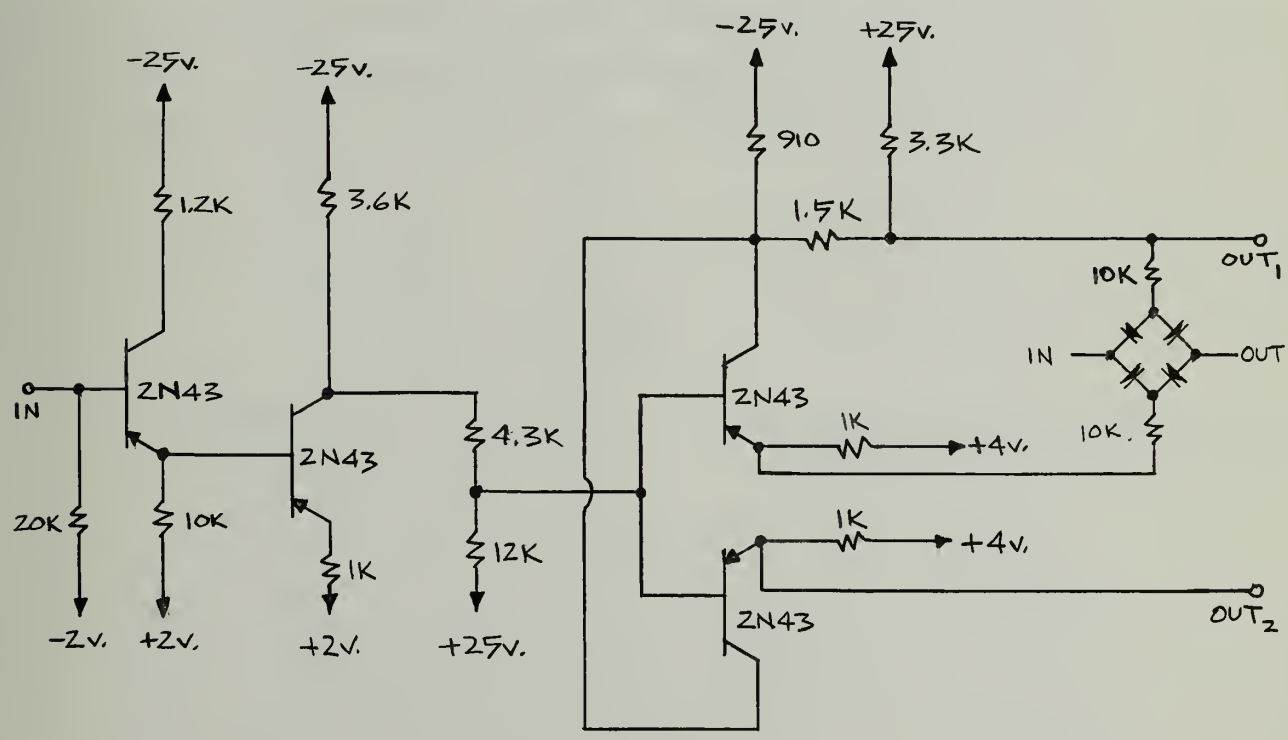
As in the preceding month much effort has been spent on the transistor test computer described in the last progress report. In particular it was found necessary to reshape the pulses coming out of the sequencing circuit by level restorers according to Figure 1. This circuit accepts pulses anywhere between $\pm$1v and $\pm$2v and brings them (under the worst tolerance conditions up to the normal $\pm$2v level. The input impedance is (as for all standard circuits) better than 10K while the load can go down to 1K without disturbing the levels. Rise times are comparable to those of the not circuit, i.e. they are somewhat less than 1μs.

It was also found desirable to design a combined gate-driver and diamond-gate unit (see Figure 2), this combination being called "gate." It happens quite often that two diamond gates are enabled or disabled simultaneously or in phase opposition. To provide for these cases, the gates have auxiliary $\pm$4v outputs which can drive another diamond gate. As can be seen



VOLTAGE RESTORING CIRCUIT

FIGURE 1



DOUBLE GATE DRIVER

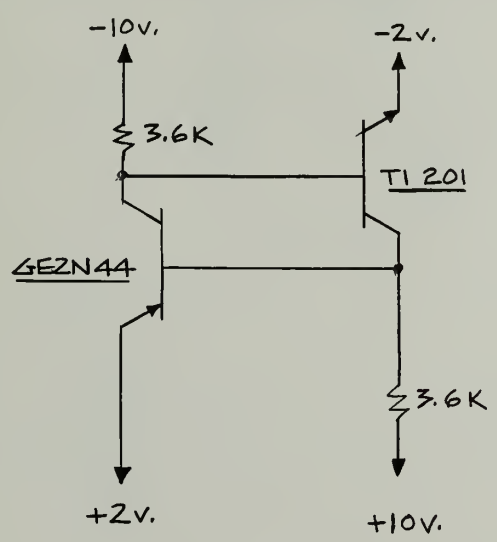
FIGURE 2

from Figure 2, the output stage uses a novel configuration: two transistors are paralleled as regards their collector but the emitters are returned separately to the bias voltage. Connecting the emitters would tend to overload the unit having the lower emitter-base resistance. It should be noticed that the equivalent collector impedance is less than 1K. The rise time for this gate was of the same order as that of the power gate driver, i.e. 1.5μs: This relatively long time is a consequence of the fact that both devices have to amplify ($\pm 2v \rightarrow \pm 4v$) and split the phase (push-pull outputs!)--this means going through two collectors.

An asynchronous counter was built, using the standard plug-in units and the above-mentioned gates. The layout is given in Figure 3. As can be seen "up" and "down" are provided for the sequencing circuit in order to make the operation asynchronous. The sequencing circuit--counter combination has worked very satisfactorily for several hours, the pulse width of the "up" pulse being about 12μs. Experiments are in progress to speed up the circuit, although this is not essential for the transistor test computer.

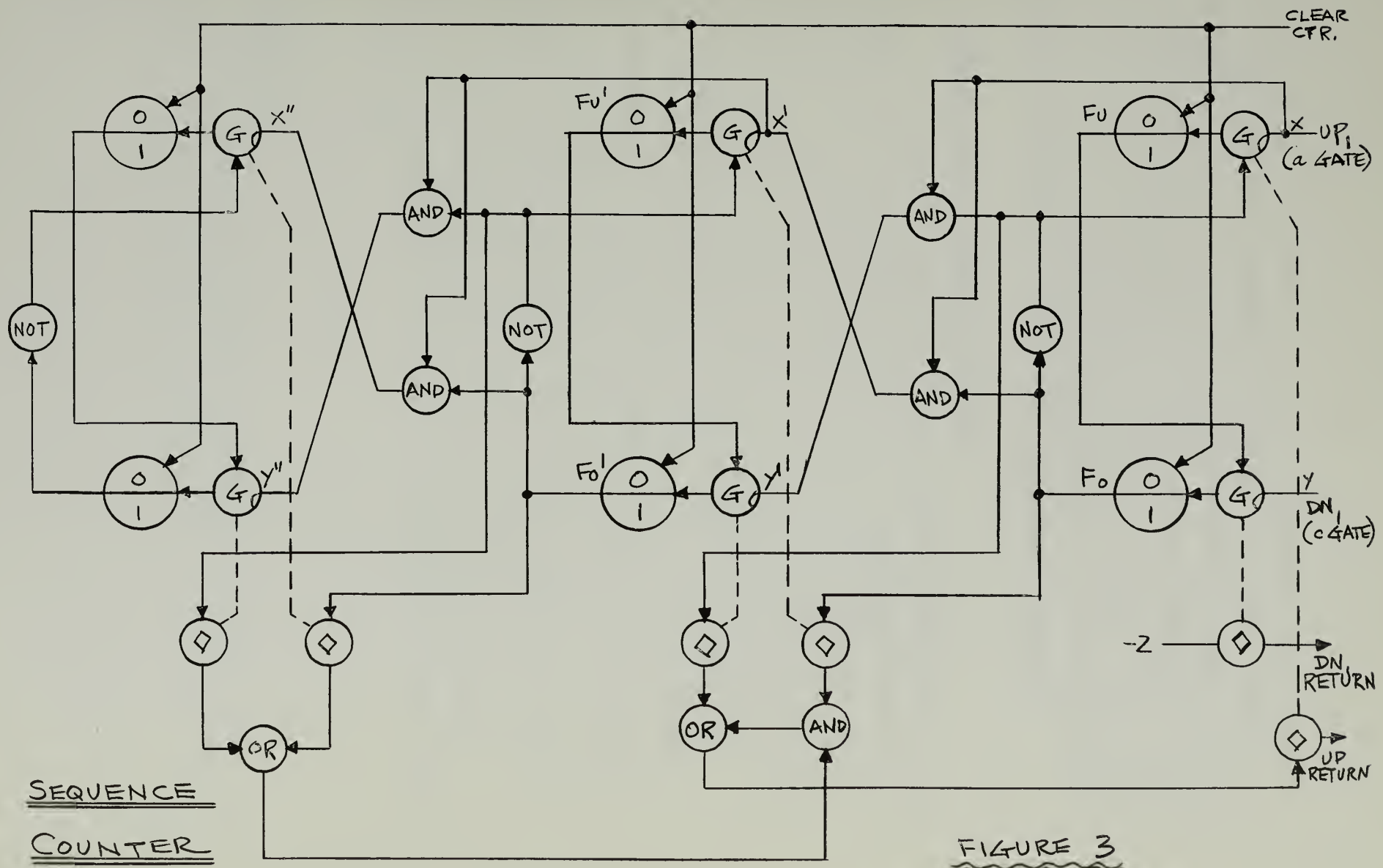
New Transistor Flipflop

A very simple flipflop, believed to be new, using only two transistors and two resistors, has been designed and tested statically. This flipflop is essentially an Eccles-Jordan using one npn and one pnp unit: Figure 4 gives the circuit values. As can be seen it has very



2 RESISTOR NPN-PNP FLIPFLOP

FIGURE 4



SEQUENCE COUNTER

FIGURE 3

surprising properties. First of all the direct returns from the emitters keep both transistors out of saturation. Secondly the swing at either collector is constant, i.e. -2v to -10v or +20v to +10v, as long as the emitter-base drop can be neglected. In order to obtain push-pull outputs with the same dc-level the circuit can be modified by the addition of zener diodes. Experiments on this as well as a racing register are now in progress. The tolerance analysis of the circuit is extremely simple and shows that variations of 20% on the supply voltages and resistance values can easily be absorbed.

Flipflop Circuit Design using Illiac

The transistor code written last month was used to find sets of circuit values suitable for high-speed flipflops. An auxiliary modification was made on the code to permit including the gate circuit tolerances in the saturation check. Several sets of values were found and two of the circuits were built into racing registers. While they operated satisfactorily as predicted by the code, they were very slow since the design used GE 2N45's. Rather small alphas were specified in the range 0.92-0.93 and 2N45's were selected for the test which had alphas in this range. It has been found by using the transistor code that both the range and actual value of alpha are important in obtaining a satisfactory design for a flipflop with reasonable tolerances on the resistors and power supply voltages. Alphas in the range 0.97-0.98 should be quite satisfactory. However these values are assumed to exist at the operating current of the circuit in question, 5-10 ma, say, rather than the 1 ma at which the alpha is specified by the manufacturer. Unfortunately, the transistors presently on hand have somewhat smaller alphas at 5 ma than at 1 ma.

VIII. CONSTRUCTION.

During the month, the drum unit was finished by the shop. This required wiring the last 72 cables between the recording heads and the preamplifiers and installing and adjusting the final covers.

Reader K has been altered in an experimental way to test several new ideas for the readers. These ideas result in a stiffer panel and an easier way to adjust the brake and clutch. Tests so far have indicated that they will tend to reduce the adjustment problems which have been present on some of the readers in the past.

IX. REPORTS AND SEMINARS.

Seminars

"Planetary Fluid Dynamics and Weather Computation" by Dr. Jule Charney, Institute for Advanced Study, January 10, 1956.

"Operation of Digital Differential Analyzers" by W. Scott Bartky, January 17, 1956.

Reports

Laboratory Report No. 68, "A Summary of High Speed Vacuum Tube Circuit Work for October and November, 1955" by Gene H. Leichner, December 12, 1955.

Laboratory Report No. 69, "Stability of a System of Equations Describing the Flow Behind a Shock," by M. Suzuki, September 15, 1955.

Laboratory Report No. 70, "Singular Shocks with Straight Branches," by Y. S. Chow, September 15, 1955.

X. PERSONNEL.

The personnel associated with the group and hence the contributors to this report are:

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REM/hc

Physics

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TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

February 1 - February 29, 1956

I. MATHEMATICAL RESEARCH AND PROGRAMMING. (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Boolean Algebra and Switching Circuits

Three theorems on the synthesis of speed-independent circuits were obtained. If we imagine the circuit to be divided into two parts A and B by arbitrarily placing some elements in A and the rest in B, then nodes may be classified as being connected to elements in A, in B, or in both. These sets of nodes may be called S_A, S_B, and S_{AB}. If the circuit formed by A and B is speed-independent and if another circuit similarly composed of parts A' and B' is also speed-independent and if S_{AB} and $S_{A'B'}$ have corresponding nodes which pass through corresponding states, then the first theorem says that the combinations A,B' and A',B are also speed-independent. The importance of this theorem lies in the fact that the circuit A,B' may be more complex than either A,B or A',B'.

The second theorem says that if A,B is speed-independent but A,B' is not, then the failure of the latter will be manifested either by different states appearing on nodes S_{AB} and $S_{AB'}$ or by a failure within circuit B'. This result should also limit the amount of testing required.

The third theorem says that if A,B and A,B' are both speed-independent and if B and B' can be represented by the same Boolean expressions, then the same state sequences appear on S_{AB} and $S_{AB'}$.

The program (outlined in the report for November) for analyzing asynchronous circuits has been written. It includes the additional feature of testing to see whether the state diagram corresponding to the circuit in question represents a distributive lattice or not. The program stores each circuit state as a word (thus requiring less than 40 elements in the circuit being tested), uses a second word to indicate which elements are excited in that state, and uses a third word for "causation" nodes which indicate which nodes may have changed so as to give immediate rise to that state. Several circuits have been tested with the program, one being a speed-independent adder and another a counter which uses only "and," "or," and "not" elements. Two versions of this program are being prepared for the library.

A version of the counter using transistors is comparable in speed and circuit complexity with conventional asynchronous counters. In terms of decision elements and complexity, the adder circuit compares unfavorably with asynchronous adders already constructed. This is largely due to the method of sensing completion, which is done by determining that each digital addition has been correctly performed rather than by sensing the completion of carry generation. Two shifting register designs indicate that a speed-independent shifting register is possible without using a great amount of additional equipment or time.

Sturm-Liouville Systems

A program has been written for testing a method of solving the Sturm-Liouville system

$$(p(x)y')' + q(x)y' + \lambda r(x)y = 0$$

$$\alpha_1 y(a) + \alpha_2 y'(a) = 0$$

$$\beta_1 y(b) + \beta_2 y'(b) = 0$$

and two sets of eigenvalues and eigenvectors have been obtained.

The method tested is not symmetric in its treatment of points near the left-hand end point and points near the right-hand end point of the interval. A method has now been found for making the method symmetric in such a way as to be computationally very convenient.

The matrices diagonalized by the process of completing the square were found to be ill-conditioned. It is hoped that the applicable routine can be rewritten soon to see if the error propagation can be alleviated. The contemplated changes would approximately double the duration of the routine, but the increased accuracy might make them worthwhile.

Continued Fractions

A rational fraction routine is being prepared. This routine will treat ordered pairs of integers as rational fractions, and its first use will be to compute the continued fraction expansion of a power series representation of a function.

Floating Address Routine

The routine has been completely written and is being checked out. One program, using 70 floating addresses, has been used in the Williams memory. What remains to be tested is the sequencing with the magnetic drum and the determination of the time required.

Miscellaneous Programs

The multiple regression routine has now been almost completely checked, the sum check being the only remaining part. An automatic eigenvalue routine, which works in a fashion similar to that of the automatic linear equation solver, has been checked. The linear equation solver for use with the magnetic drum has also been checked, and it is necessary only to solve a large set of equations to obtain timing information. It is expected that this routine will be much faster than the previous drum linear equation solver, which required about 40 minutes (exclusive of input) to solve a set of 96 equations.

II. ANALYTICAL PROGRAM. (This work is supported in part by National Science Foundation Grant G-1221.)

A study of the gravitational field equations in a spherically symmetric space time where the field is due to a perfect fluid has begun. It was shown that, as in the plane-symmetric case, for isentropic flow, the field equations imply the conservation of mass. The static field equations reduce to a set of ordinary differential equations which are being written in a form for suitable numerical solution by Illiac. It is planned to study a variety of fluids, each described by a different caloric equation of state and to obtain numerical solutions for their gravitational fields when they are in static equilibrium.

The approximate procedure for dealing with general solutions of the Einstein field equations inside a region of space-time occupied by a plane-symmetric distribution of a perfect fluid leads to a set of linear equations

for the higher order corrections to the gravitational field quantities when the zeroth order approximation is taken to be the solution of a corresponding problem in special relativity. These equations have been written in terms of the special theory of relativity characteristic variables and have been reduced to a form where numerical procedures can be readily applied.

III. MACHINE USE

During February specifications were presented for 23 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 741. Numbers followed by T are for theses.

741 Computer. Continued Fraction Expansions. This program is designed to find the continued fraction expansion of a function when the power series expansion is given.

742 Food Technology. Effect of Processing and Storage Factors on the Quality of Strawberry Preserves. The analysis is carried out by calculating variances and covariances which involve four factors and nine determinations on 120 samples.

743 Computer. Determination of Flow Behind Shocks. This problem is concerned with the solution of a set of partial differential equations arising in the study of shocks in hydrodynamics.

744 Industrial Relations Center, University of Chicago. Definition and Measurement of Employee Morale. This is a statistical analysis in which a study will be made of the definition of five factors of morale in terms of simply-framed questions, understandable to the average industrial employee. The procedures used will involve calculation of product moment correlations and rotations.

745 Food Technology. Measures of Supply Determinants for Various Animal Fats. This is a supply study which will complement an earlier study on the demands interrelationships for selected fats and oils. Multiple regression techniques will be used.

746 T Structural Research. Frequency Analysis. Library Routine M-5, for solving the equation $A - \lambda B = 0$ will be used to determine frequencies of tall stacks which may develop severe aerodynamically excited oscillations.

747 Electrical Engineering. Antenna Spacing Error. The problem is concerned with the evaluation of a trigonometric expression which is calculated by direct methods using Library Routines T-4 and T-5.

748 Electrical Engineering. Fourier Analysis of Error Data. Calibration errors of a four-element Adcock direction-finding antenna by the library Fourier analysis routine, V-4 for thefirst 18 harmonics are found.

749 Dairy Science. Sampling Errors of the Genetic Correlation. Observations on three different production traits, namely milk yield, fat percentage and fat yield have been collected on approximately 30,000 parents and daughters from approximately 4000 dairy herds. A statistical analysis will be carried out.

750 Physics. Calculation of Energy Release as a Function of Temperature. This is a data-processing problem in which the rate for release of energy from copper worked at liquid nitrogen temperature is determined with respect to temperature as the system warms up from about -186°C to about +25°C.

751 MURA. Characteristic Exponent Tables. The problem consists of solving the four parameter differential equation and calculating certain constants from the solutions for various values of the parameters.

752 Agricultural Economics. Productivity Trends in Agricultural Resources. Multiple regression techniques will be used to estimate changes in the productivity of certain classes of agricultural resources over the 18 year period 1936 - 1953. Data from 146 farms which had continuous records over this period will be utilized. Trends observed in such things as labor productivity, land productivity, etc. will be used for suggesting desirable changes in resources in Illinois agriculture.

753 Astronomy. Non-adiabatic Pulsations of a Stellar Model. The problem of pulsating stars is essentially that of the radial oscillations of the gas sphere so that the pressure, density and temperature are functions of the radial distance in time only. In this problem, a system of partial differential equations governing them is reduced to a non-linear differential equation which is integrated numerically.

754 T Chemistry. Distribution in Restricted Random Walk. This problem is concerned with finding a distribution function for a restricted random walk. This function is known for the unrestricted walk (Gaussian) and it is important to know whether or not it is also Gaussian for restricted walks.

755 Psychology. Factor Structure in Six Year Olds. This study consists of a series of factor analyses on matrices varying from 80 x 80 to 110 x 110. Each extraction will be followed by oblimax rotation and by matrix multiplication for rotations examined visually from photographic data obtained with the cathode ray tube output.

756 Psychology. International Second-Order Humor Factoring. This study consists of a series of about 12 centroid factors analyses mostly on 44 x 44 phi coefficient matrices, calculated on about 170 subjects. Extimation of factor scores for several hundred subjects will be carried out, weighing each score 0, 1, or 2.

757 Computer. Circuit Test for Speed-Independence. This is a program for determining the speed independence of asynchronous circuits. The user describes the circuit and supplies an initial state, along with other information determining output and stopping of the test. The program then computes successive states for speed-independence.

758 Economics. The Estimation of Annual Rates of Productivity Changes for Selected Industries. The objective of this problem is to compute annual rates of growth for five different measurements of productivity. This will be done for twenty different industries over the period 1919 - 1940. Multiple correlation analyses will be carried out.

759 Structural Research. Moment Distribution. The problem is to distribute the unbalanced moment at any or all joints of a multi-storied frame to individual frame members by the Hardy Cross method of moment distribution. The maximum permissible number of joints including column bases will be 100.

760 Economics. Estimates of Parameters in Economic Models under Various Controlled Conditions. Library Routine K-2 will be used to calculate means, variances, co-variances for a considerable number of paired variables. The general problem is one of examining parameter estimates in economic models made up of stochastic equations.

761 Bureau of Educational Research. Agreement Matrix. The matrix given here is a 38 x 38 matrix which represents agreements among judges, and the Illiac will be used to raise it to 2nd, 3rd, or 4th powers.

762 T Psychology. Study of Mathematical Reasoning. Certain Styles of mathematical reasoning have been defined. A test was administered by the Illinois High School Testing Bureau to 400 students, and has been analyzed by people experienced in mathematics to determine which styles of reasoning were used for the problems. A pattern analysis technique will be used to evaluate the data.

763 Chemistry. Crystal Field Extension. The problem is concerned with the calculation of change in energies of cupric ion 3d orbitals surrounded by a charge distribution of D_{4h} symmetry. The solution involves integrations over space.

Table I shows distribution of machine time for the month of February.

TABLE I

Regular Maintenance and Illiac Engineering	49:41
Unscheduled Maintenance or Repair	10:58
R.A.R.	6:23
Drum Engineering	64:10
Leapfrog	43:49
Wasted	:03
<u>Use by Departments</u>	
Computer Group	12:54
Physics	47:05
Control Systems Laboratory	79:54
Structural Research	6:06
Structural Research (AF 24994)	6:30
Structural Research (AF 170 T-POT)	:03
Theor. and Applied Mech. (N6ori-07135)	4:51
Electrical Engineering	1:06
Electrical Engineering (Nobs 64723)	1:09
Psychology	10:19
Psychology (MD 569)	:43
Electrical Engineering (AF 3220)	5:41
Chemistry	23:59
Agriculture	8:44
MURA	109:30
Institute of Communications Research	2:49
University of Chicago	1:12
Demonstrations	2:23
Classes	:59
Miscellaneous	11:30
Total	512:31

IV. ERROR FREQUENCY AND ANALYSIS.

The machine is normally used for "engineering" and maintenance between 8:00 A.M. and 12:00 N, and for a check of its performance between 6:00 and 6:30 P.M. of each weekday. Since the periods between 8:00 A.M. and noon, together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between noon and 8:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between noon and 8:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 6:00-6:30 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This overall system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for February.

TABLE III

Arithmetic Unit	0	Reader Control	0
Control	0	Input Output Control	0
Reading combined with punching	2	Fuse blew in Ckt. #23	1
Reading only	13	Fuse blew in Ckt. #12	1
Punching only	5	Unknown	2
Memory	3	Operator Error	1
			28

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
2/1/56	17:05	2:55	3	(1) Fuse blew in circuit 23. (2) Fuse flew in circuit 12. (3) Evidently Reader K error.	:00	2:22	0
2/2/56	19:59	:01	1	(1) Reader H error.	:00	1:23	0
2/3/56	19:59	:01	1	(1) Reader K error.	:00	:46	0
2/6/56	19:59	:01	1	(1) Light on Reader K burned out.	:00	1:49	0
2/7/56	19:46	:14	2	(1) Unknown, but possibly reading error with Reader H. (2) Unknown.	:00	1:22	0
2/8/56	20:00	:00	0		:00	1:30	0
2/9/56	20:00	:00	0		:00	1:12	0
2/10/56	19:21	:39	1	(1) Failed in 2^{-35}, probably memory	:00	1:11	1
2/13/56	20:00	:00	0		:00	1:06	0
2/14/56	19:59	:01	1	(1) Reader K failure.	:00	1:03	0
2/15/56	19:58	:02	2	(1) Punched "L" instead of "S". (2) Same as (1).	:00	1:16	0
2/16/56	19:08	:52	2	(1) Memory 0 → 1 position 2^{-25}; replaced cathode ray tube 25 (2) Light on Reader K out.	:00	1:28	2
2/17/56	19:55	:05	1	(1) Screw came out of motor coupling on Punch No. 5.	:00	:40	0
2/20/56	20:00	:00	0		:00	1:20	0
2/21/56	17:30	2:30	3	(1) Error during reading with large reels. (2) Error during reading with large reels. (3) Probably punch No. 3 error.	:00	2:17	1
2/22/56	16:08	3:52	7	(1) Order pair printout routine omits 0 on every LO order. Reason unknown. (2) Reader K error (3) Special leapfrog input-output failure "H" gate on C.F. bad.	:00	:39	2

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
2/22/56	(Cont.)			(4) Reader K error. (5) Reader K error. (6) Reader K error. (7) Operator error.			
2/23/56	19:08	:52	2	(1) Changed spring on "4" hole armature of Punch No. 5, changed light in "A" gate. (2) Two different results with same tapes.	:00	1:42	0
2/24/56	19:16	:44	1	(1) Leapfrog, possibly 2^{-11}.	:00	:52	1
2/27/56	20:00	:00	0		:00	1:07	0
2/28/56	20:00	:00	0		:00	:56	0
2/29/56	20:00	:00	0		:00	1:00	0
Totals	407:11	12:49	28		:00	27:01	7

V. COMMENTS ON ILLIAC DRUM MEMORY

Trouble-shooting of the drum storage unit continued during the month of February. Major difficulties encountered included the following:

1) Oscillations were observed on the cathode busses of the record tubes. The oscillations were traced to the +300 volt supply and were eliminated by 0.01μfd bypass condensers on the +300v supply in the 815 record amplifier driver chassis.

2) It was found that playback switching transients were causing errors during transfers from the drum. It was found that the time constants in the switching smoothing circuits were twice as large as they should have been. Condensers of the correct value were installed to eliminate such errors.

3) The drum test code was rewritten so that every third word was consulted rather than every fifth, with the effect that the drum was consulted more frequently and that switching transients were more severe. Addresses from which switching was made were also randomized. It was found that switching from mythical tracks (numbered 320 to 3LN) caused errors. These errors were eliminated by increasing the minimum level of the switch busses. The switch busses are at this minimum level during selection of a mythical track.

4) It was observed that the phase of played back signals varied by as much as two microseconds from one track to another. The phase shift is due to both variations among heads and to differences in length of cables between the heads and the record tubes. At the end of the month, methods of correcting for this phase shift were being investigated.

VI. RESEARCH ON COMPUTER COMPONENTS

(This work is supported in part by the Office of Naval Research under Contract N6ori-07124.)

Transistor Test Computer

The work on the transistor test computer has continued as our priority project while we are waiting for faster and more stable transistors. The transistor test computer uses circuits with operation speeds of about 1 microsecond and is being assembled to obtain experience in the use of

transistors. It will contain an arithmetic unit of four binary digits, a small control which will make it possible to carry out additions and multiplications and a small memory to enable a test routine to be carried out. The memory will be of four words of six bits each. The layout of the chassis has been determined and work on them has started already.

The core memory circuits were redesigned in order to take account of the tolerance conditions and also to simplify the circuitry involved. In particular a readout-amplifier has been designed (see Figure 1) which uses 3 ac-coupled stages, a dc-coupled amplifier stage and a dc-coupled emitter-follower. The total amplification is about 220. The pulse is clipped at the output to +2V and -2V by the emitter-follower bias and a diode respectively. The amplifier exhibits rise and fall times of less than 1 microsecond, the base-width of the pulse being 3 microseconds. Figure 2 shows the input and output for a "1" signal and a "0" signal coming from the core matrix.

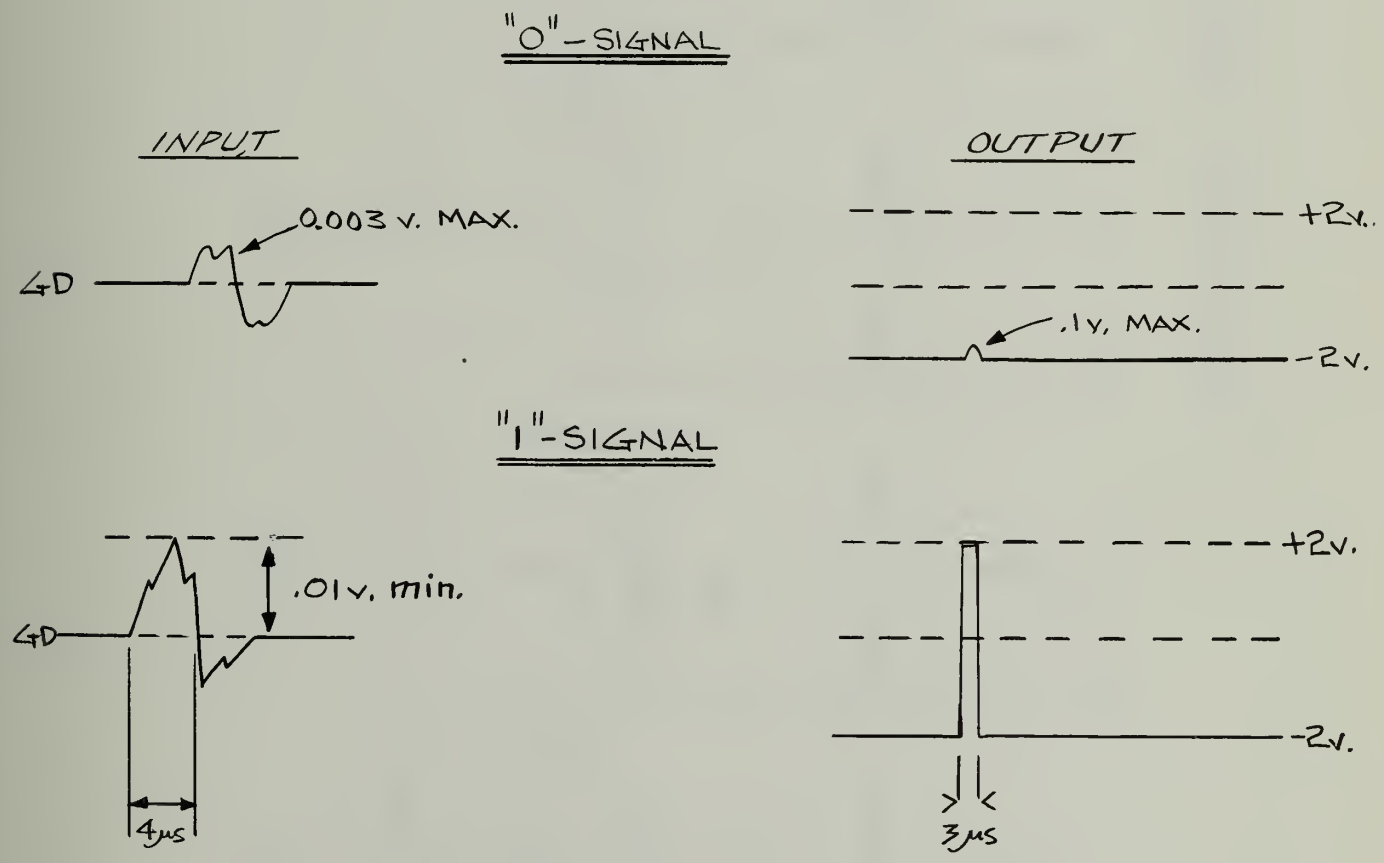
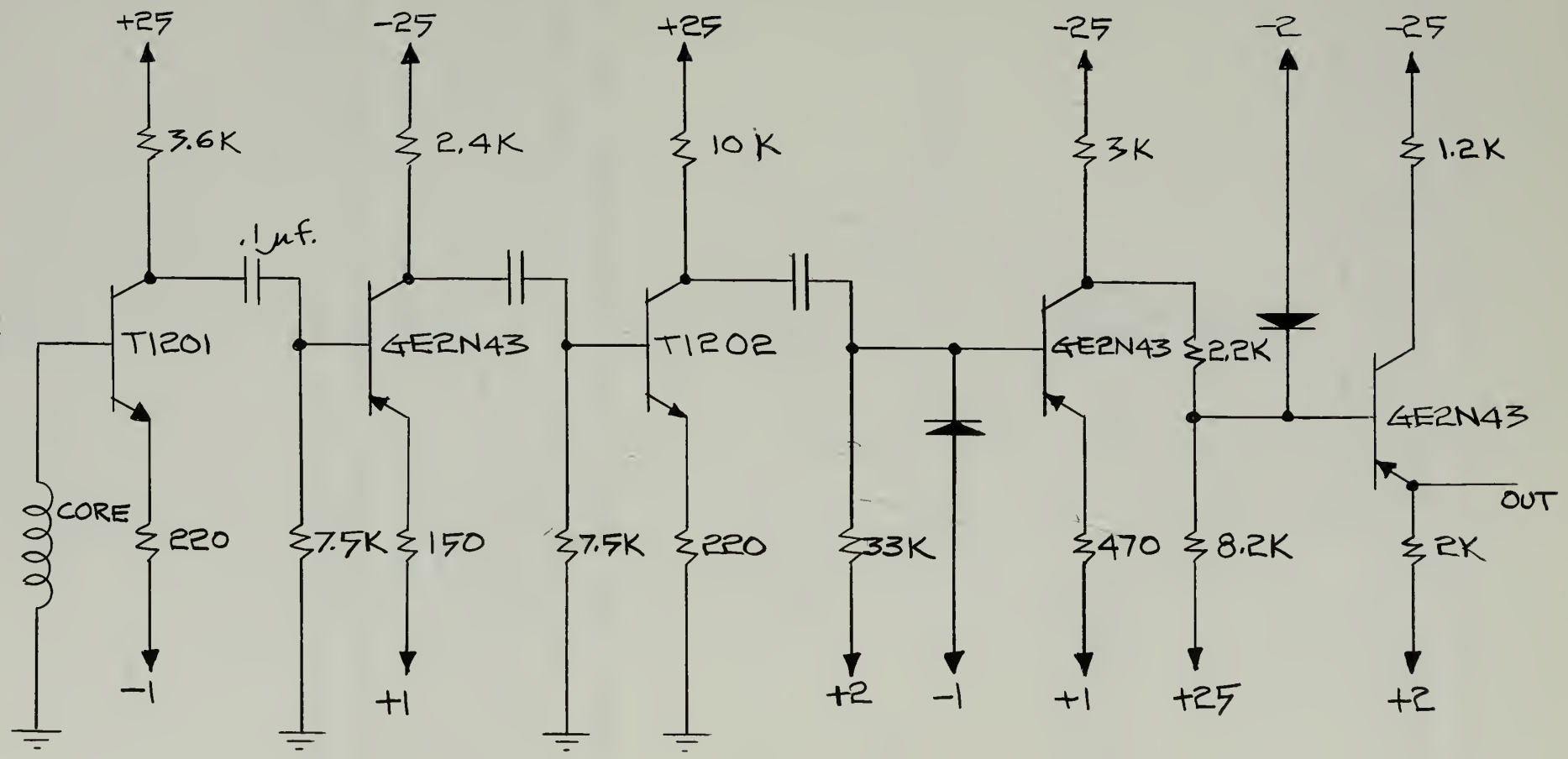


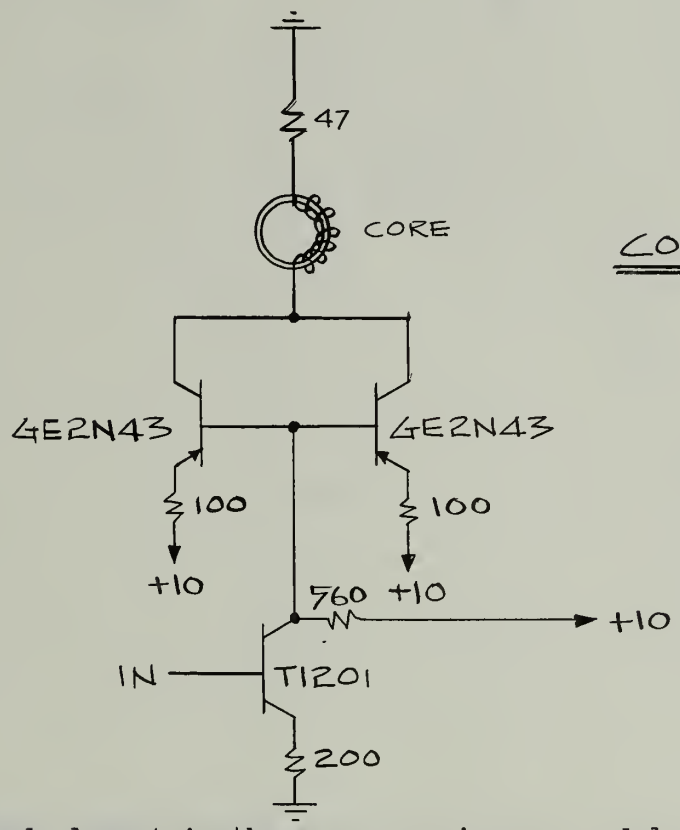
FIGURE 2



READ OUT AMPLIFIER

FIGURE 1

A new core driver according to Figure 3 was designed and tested. The version shown below furnishes 100 ma-pulses (rise time ~1 microsecond, amplitude 4V), but if necessary a slight modification allows one to draw 200 ma. This 3 transistor unit replaces a former 7 transistor unit.



CORE DRIVER

FIGURE 3

The third element in the memory-series was a delay element which delays the read-return pulse by 5 microseconds. Figure 4 shows the layout. The first stage uses an RC-network in the collector to produce an exponential waveform; the collector is kept out of saturation by a diode. The second stage senses a critical level and when this is attained it goes very rapidly into saturation: saturation guarantees a minimum length of the return pulse. After the usual clipping the pulse goes out through an emitter-follower. The unit is designed in such a fasion that the rise time of the return pulse is kept below 1 microsecond.

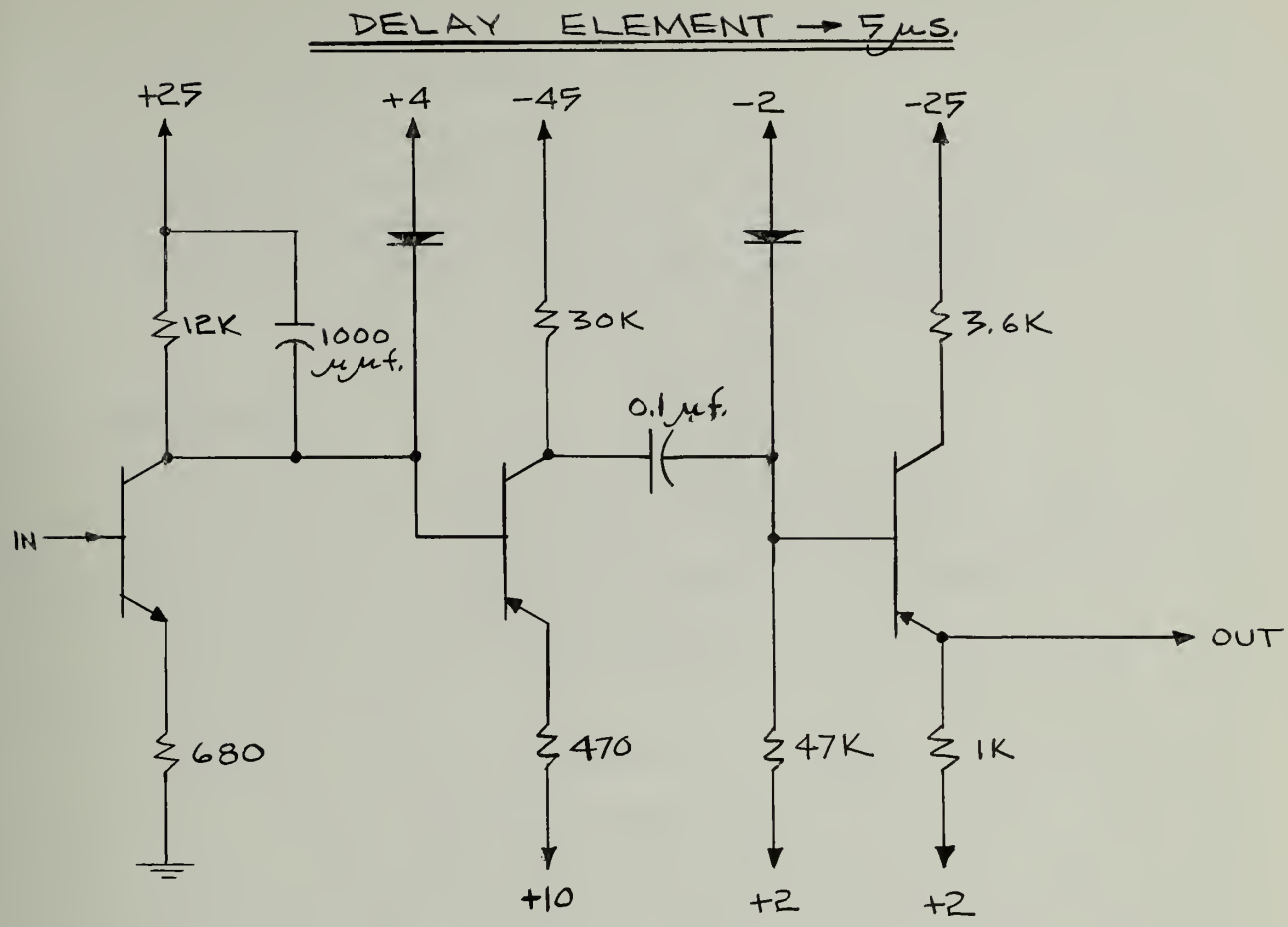


FIGURE 4

New Transistor Circuits

Some time was spent on the theoretical and experimental investigation of the 2-resistor npn-pnp flipflop described in the last issue of the report. Our goal is to have more complete control over the high-current condition in the transistors in the "on"-state.

A new project has been started to study the use of solid-state delay-lines as memory elements (used in a serial fashion). A pulser giving 20 microsecond pulses was designed and built and some preliminary experiments on the usefulness of power-transistors as delay lines made. Equipment was set up to repeat the experiment of Haynes and Shockley on drift mobility: this can be developed into a memory device.

Some tests have also been made on coaxial delay-line memories for a short fast memory.

Fast Transistor and Diode Pulse Tester

A pulser has been designed to test the transient phenomena of transistors and diodes in intervals of 10 or 20 millimicroseconds. The pulser, using EFP60 tubes, produces pulsations with total rise and fall times of 10 millimicroseconds and with pulse lengths which are adjustable.

VII. CONSTRUCTION

A reperforator unit for the Teletype Room, using a 60 character per second punch operating from a photoelectric tape reader is being constructed. Chassis corresponding to Drawings M643 and M640 have been completed and that corresponding to Drawing L644 has been started.

The memory test rack has been moved from the Circuits Laboratory to the Electronics Laboratory.

Additional work has been carried out to improve the photoelectric tape readers. Ten cast aluminum boxes have been received and have been machined in part. These boxes, since they are more rigid, will tend to hold the adjustments of the photoelectric tape readers for a longer period of time.

VIII. REPORTS AND SEMINARS

Seminars

"Test of an Inventory Control System on Ferut" by Professor C. C. Gotlieb, University of Toronto, February 14, 1956.

"The Use of Controlled Random Number Processes for Composition of Music in the Illiac," by R. A. Hiller and L. M. Isaacson, February 28, 1956.

IX. PERSONNEL

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate (started Feb. 1)
Bartky, W. Scott, 1/2 time Res. Asst.
Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
Clements, Virgil F., Jr. Laboratory Mechanic
DeWit, Roland, 1/2 time Res. Asst.
Ehmen, Mrs. M. Gwendolyn, Computer Teletype Operator
Farrington, Carl C., 1/2 time Res. Asst.
Fishel, Jerome H., 1/2 time Res. Asst.
Goldberg, Jack L., 1/2 time Res. Asst.
Golub, Gene H., 1/2 time Res. Asst.
Holm, Walter H., Jr. Electronics Technician
Hill, Robert S., Computer Operator I (started Feb. 8)
Huffman, Wm. L., Computer Operator II
Kerkering, Thomas E., Sr. Laboratory Mechanic
Krabbe, Shirlie P., Sr. Electronics Tech. for Illiac
Leichner, Gene H., 3/4 time Res. Asst.
Lopeman, Harold E., Electronics Engineer for Illiac
Lurie, Fred M., 1/2 time Res. Asst.
Lytle, Harold R., Jr. Electronics Tech. (started Feb. 20)
Martin, Ronald D., Jr. Electronics Tech. (resigned Feb. 17)
Meagher, R. E., Chief Engineer
Metze, Gernot A., 1/4 time Res. Asst.
Michael, G. W., Administrative Assistant
Miller, Raymond E., 1/2 time Res. Asst.
Morrill, Ronald F., Draftsman
Muller, David E., Res. Asst. Prof. of Applied Math.
Nash, J. P., Res. Prof. of Applied Math.
Nelson, James C., 1/2 time Res. Asst.
Newmark, N. M., Chairman, Executive Committee
Pelg, Edmund, Jr. Electronics Technician
Peterson, Donald A., 1/2 time Res. Asst. (started Feb. 1)
Poppelbaum, W. J., Res. Asst. Prof.
Ray, Sylvian R., 1/2 time Res. Asst.
Robertson, James E., Res. Asst. Prof. of Elec. Eng.
Russell, Miss Ramona J., Computer Operator I
Seshu, Mrs. Lily H., 1/2 time Res. Asst.
Stephens, Allen F., Jr. Laboratory Mechanic
Taub, A. H., Res. Prof. of Applied Math.
Warner, John J., Computer Operator I (resigned Feb. 10)
Wenta, Joseph M., Sr. Electronics Technician
Wier, Joseph M., Research Associate (resigned Feb. 22)
Yu, Hwa-Nien, 1/2 time Res. Asst.

Student Assistants

Dean, Floyd R.
Geis, John P.
Goodman, Robert
Kirwan, John F.
Ogata, Albert I.

The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

J. P. Nash

J. P. Nash

REM/hc

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

March 1 - March 31, 1956

I. MATHEMATICAL RESEARCH AND PROGRAMMING. (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Theory of Speed-Independent Circuits

A number of theoretical results have been obtained concerning speed-independent circuits which may have considerable bearing on the problem of circuit synthesis. These results fall into two classes; first, results which depend upon the consistent logical behavior of decision elements during the action of the circuit, and second, results that apply only to distributive circuits.

1. In the first class of results it has been shown that the C-states which are equivalent to a given I-state may be represented by the formula

$$S + \sum_{i=1}^{k} a_i v_i$$

where S is a C-state and $v_1, v_2, \ldots, v_k$ is a set of k vectors which are characteristic of the I-state. The coefficients a_i are non-negative integers which may otherwise be chosen arbitrarily--any choice giving a C-state equivalent to the same I-state as S and any such C-state conversely yielding a set of coefficients. The addition occurring in the above formula is numerical, vector addition. It has furthermore been shown that the non-zero components of the vectors $v_1, \ldots, v_k$ are distinct in speed-independent circuits. Each vector may therefore be said to "cover" the set of nodes for which it has non-zero components.

During the action of a circuit no vectors in the set $v_1, \ldots, v_k$ are lost but new vectors may be added to the set. The number k is therefore a characteristic number connected with the I-state which can never decrease during the operation of the circuit. One can also show that the nodes covered by any vector v_i operate independently of the other nodes of the circuit and may be regarded as a separate machine. If such a separation is made for each of the vectors v_i we obtain k separate machines each with all its nodes covered by a single vector and hence having k = 1. Such machines cycle indefinitely and can never yield additional vectors. They also have the property that if any node within them is broken they will stop. If any nodes in the original circuit have no vector covering them, this set of nodes represents a machine having k = 0. Such a machine may yield additional vectors during the action of the circuit.

By using the separation theorem we see that the properties of all machines may be studied by studying the above two types. Rules have been obtained for predicting the vectors v_i for circuits which are formed as combinations of these types when the combinations are those described in Digital Computer Laboratory Report 66.

2. The second class of results applies specifically to distributive circuits. There is a result due to G. Birkhoff to the effect that there is a one-to-one correspondence between distributive lattices L satisfying the descending chain condition and partially ordered sets P satisfying the descending chain condition. (All lattices corresponding to circuits satisfy the descending chain condition.) The elements of P are isomorphic with the join-irreducible elements of L. Any element of L may be expressed in a unique, irredundant way as the join of such elements. Such an expression is analogous to the canonical expansion in Boolean algebra.

Now it is also possible to show that if the lattice L represents the state diagram of a distributive circuit, then the elements of P correspond to the signals appearing in the circuit. (A signal may be mathematically defined as a pair of numbers (a,i) provided some C-state exists whose ith component is a, i.e. a changes have occurred at the ith node.) A causative relation exists among signals which is defined as follows: We write (a,i) causes (b,j) if for all states having signals (a,i) and(b,j) $a' < a$ implies $b' < b$. This ordering can be shown to be equivalent to the ordering defined in Birkhoff's theorem.

This ordering defines a covering relationship which has the following property: (b,j) covers (a,i) if and only if there exists a pair of states S_1 and S_2, S_1 with signals (a-1, i) and (b-1,j) having i excited and j in equilibrium, and state S_2 directly following S_1 in which signals (a,i) and(b-1,j) exist with j excited. This result together with the definition of causation allows us to predict the excited nodes in any state from the structure of P and hence the lattice may be constructed.

The importance of these results lies in the fact that the partially ordered set P of signals is much simpler than the state diagram as regards structure and number of nodes. Its use in place of the state diagram would have these advantages:

1. A simple representation of the action of the circuit would be given by P.

2. The circuit obtained from this diagram would be distributive and hence speed independent.

3. There is a much closer correspondence between the diagram of P and the circuit it represents than between the state diagram and the circuit. Each node of P, in fact, corresponds to a decision element in the circuit.

Logical Design of Speed-Independent Circuits

Work has continued on efforts to design a control unit for a speed-independent computer which will utilize already designed addition and shifting components. It has been found possible to control the operations of adding and shifting units with a pseudo-clock constructed out of dual flipflop scale-of-two counters. One question which arises concerns the desirability and possibility of placing all operations under the control of one such pseudo-clock which would then sequence all operations except that of the control of which it is a part. This would eliminate the necessity for having other independent flipflops change state at every step of the arithmetic process as is required in some techniques of control design.

Continued Fraction Expansions

With the essential arithmetic details completed on the program for rational fractions, investigation is continuing on other applications of continued fraction techniques. These include matrix inversion for matrices with rational elements, inversion of power series, and expansion of functions in Taylor's series and Fourier series with exact rational coefficients.

Drum Bootstrap and Playback Routine

This program is now functioning properly, although a few details remain to be completely checked. When the order pair 85 00S 40 000 is set up in the order register, this routine pulls itself into the Williams memory, occupying locations 0 through 6 and 1015 through 1023. It will then bring any one of 16 routines stored on the drum into the fast memory and transfer control to that routine. When used in conjunction with the Combined Drum Post Mortem Routine, this program will first dump the contents of the Williams memory on the drum before calling for the post mortem routine.

Sturm-Liouville Systems

The approximation used in solving the Sturm-Liouville problem $(py')' + qy + \lambda ry = 0$ with homogeneous boundary conditions leads to the matrix equation $Ay = \lambda By$ where A and B are symmetric and B is positive definite. The computations have been rearranged so that A and B are now of the form

$$\sum_{i} \sum_{r,t} \alpha^{i}_{j,r} \quad P^{i}_{r,t}$$

This has necessitated writing two new routines. The routine for generating the α^{i}_{jr} matrices has also been rewritten so that only integer operations are involved. With this routine there is no longer any generated or propagated error.

Results of a few preliminary trials seem to indicate that the matrix B becomes ill-conditioned as higher order approximations are attempted. Consequently the scope of the tests to be run has been enlarged so as to include a more systematic study of the round-off error as a function of the order of approximation and the mesh size.

Miscellaneous Programs

The linear equation solver which uses the magnetic drum is being modified so that sum checks are stored on each row when transfers are made to the drum.

II. ANALYTICAL PROGRAM. (This work is supported in part by National Science Foundation Grant G-1221.)

Work is underway on a code to integrate the Einstein gravitational field equations for a static spherically symmetric case where the field is due to a perfect fluid. The field equations have been reduced to a set of ordinary differential equations which will be solved by the Runge-Kutta method. The method used will allow the caloric equation of state of gas to be prescribed or will allow an arbitrary relation between the pressure and the rest energy density to exist.

Further progress has been made on the approximate procedure for dealing with general solutions of the Einstein field equation inside a region of space-time occupied by a plane symmetric distribution of a perfect fluid. The relations existing between the co-moving coordinate system, in terms of which the problem may be formulated, and a general coordinate system in the space-time have been studied. It has been shown that whereas the equations describing the behavior of the gravitational and fluid properties of the field have the sound cone as a set of characteristics, the equations describing the coordinate transormation have the light cone as a set of characteristics.

III. PROGRAM LIBRARY.

The following program has been added to the library.

P-15 (207) Multiple Precision Integer Conversion. 32 words. This is a closed routine with two program parameters which is designed for converting multiple precision binary integers to decimal form. There is no restriction upon the number of memory locations occupied by the binary integer. The coefficients of the converted decimal integer (other bases may also be used) can be printed with a standard 11-place integer print routine.

IV. MACHINE USE.

During March specifications were presented for 9 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 764. Numbers followed by T represent thesis problems.

764 Dairy Science. Inbreeding Equations. This problem estimates inbreeding coefficients through the solution of simultaneous linear algebraic equations.

765 Psychology. Nursery Factoring. This problem is concerned with the analysis of test data on 80 small children in a nursery school. Three correlation matrices

will be factored by the centroid method, rotated by the quartimax method to simple structure, and then further rotated visually by plotting and photographing results on the cathode-ray tube output.

766 Agronomy. Preparation of a Random Sequence of Integers. Library Routine V-3 will be used to produce a table of integers.

767 T Psychology. Linear versus Configural Prediction of Scholastic Performance. This is a statistical analysis to determine whether non-linear and/or joint functional relationships exist between a complex criterion (academic success) and a set of 8 independent behavioral measures widely varied as to psychological content. The calculation will involve calculation of a matrix of product-moment correlation coefficients, use of the linear equation program to obtain beta weights, and use of the product-moment routine to obtain configural validity coefficients.

768 T Social Work. Personality Structure of Service and Non-Service Children. Data have been collected on a group of 8th grade children from families both in and not in the military service. The purpose of the study is to see whether there is a significant personality difference.

769 Iowa State University Physics Department. Computation of Table of Doversines. The program computes doversine x (i.e., $2(1 - \cos x)$) and log doversine x.

770 Geology. One-Dimensional Fourier Synthesis. In a problem concerned with an electron density distribution in centrosymmetrical sheet silicates, use is made of Fourier expansions. In this case summations of a Fourier series are desired.

771 Psychology. Farm Supply Study. A factor analysis will be made for a system of 86 variables which are to be used as criteria of successful operations of 32 cooperatives in a study of the relationship of interpersonal perception scores to the success of decision-making groups.

772 Computer Laboratory. Solutions of Hydrodynamic Systems. The static solutions of isentropic hydrodynamic systems in spherically symmetric space-times will be obtained by integrating Einstein's field equations for various types of gases.

Table I shows the distribution of machine time for March.

TABLE I

Regular Maintenance and Illiac Engineering	49:03
Unscheduled Maintenance or Repair	63:41
Drum Engineering	74:36
R.A.R.	8:25
Leapfrog	58:27
Wasted	1:30
<u>Use by Departments</u>	
Computer Group	16:48
Physics	62:12
Control Systems Laboratory	42:05
Structural Research	13:09
Structural Research (AF 24994)	3:27
Structural Research (AF 170 TEAPOT)	2:34
Theor. and Applied Mech. (N6ori07135)	:12
Psychology	15:40
Electrical Engineering	2:35
Electrical Engineering (AF 3220)	1:54
Chemistry	20:07
Agriculture	11:06
MURA	100:48
Inst. of Communications Res.	4:06
University of Chicago	:33
Iowa State University	:24
Demonstrations	11:08
Miscellaneous	11:17
Total	575:47

V. ERROR FREQUENCY AND ANALYSIS.

The machine is normally used for "engineering" and maintenance between 8:00 A.M. and 12:00 N, and for a check of its performance between 6:00 and 6:30 P.M. of each weekday. Since the periods between 8:00 A.M. and noon, together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between noon and 8:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between noon and 8:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 6:00-6:30 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This overall system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for March.

TABLE III

Arithmetic Unit	0	Reader Control	0
Control	0	Input Output Control	1
Reading Combined with Punching	0	Blown Fuse, Ckt. 23	1
Reading only	6	Memory	3
Punching Only	1	Unknown	1
			13

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
3/1/56	20:00	:00	0		:00	1:37	0
3/2/56	20:00	:00	0		:00	1:09	0
3/5/56	20:00	:00	0		:04	:55	0
3/6/56	20:00	:00	0		:00	1:03	0
3/7/56	20:00	:00	0		:00	:58	0
3/8/56	20:00	:00	0		:00	:47	0
3/9/56	20:00	:00	0		:00	1:07	0
3/12/56	20:00	:00	0		:00	:48	0
3/13/56	19:44	:13	1	(1) Light on Reader K burned out.	:03	1:03	0
3/14/56	19:18	:42	1	(1) Error due probably to reading.	:00	1:02	0
3/15/56	20:00	:00	0		:00	1:22	0
3/16/56	19:52	:08	1	(1) Punch No. 4 not punching clean holes.	:00	:47	0
3/19/56	20:00	:00	0		:00	1:04	0
3/20/56	18:24	1:36	2	(1) Memory failure 2^{-17}. (2) Bad tubes in tape punch control.	:00	1:09	2
3/21/56	19:59	:01	1	(1) 24 changed to a 25 order. (Single-Digit error.	:00	1:23	0
3/22/56	20:00	:00	0		:00	:50	0
3/23/56	19:52	:08	3	(1) Reader K not operating properly. (2) Reader H did not stop tape properly. (3) Probably Reader K error.	:00	:53	1
3/26/56	:21	19:35	1	(1) Memory error; apparently began with two blown fuses. This error happened intermittently, about once every two hours. It was looked for for several days without success. After eight cathode ray tubes were changed on April 10, the error did not occur again. The time looking for this error is reported as repair time during the next 11 running day. This error is reported only once.			

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
3/27/56	4:51	15:09	0		:00	3:09	0
3/28/56	4:15	15:45	2	(1) Bulb burned out in reader. (2) Blown fuse, circuit 23.	:00	1:39	0
3/29/56	8:30	11:30	0		:00	:48	0
3/30/56	16:01	3:56	1	(1) Changed CRT Chassis. (Memory error)	:03	6:13	1
	371:02	68:48	13		:10	30:07	7

VI. COMMENTS ON ILLIAC AND RELATED FACILITIES.

Auxiliary Drum Memory

During the month, the drum storage unit was available for code checking and production on a limited basis. The most important difficulties included the following:

Date	Track	Nature of Trouble
March 2	OIN	Bad solder connection
March 2	254	6AU6 screen grid short
March 6	All	6AK5's. A delay pulser
March 7	Group N	815's in track OL8
	2IN	2C51 low g_m
	318	815's
	OnO	6136 K-filament leakage
March 8	314	815's low emission
March 14	ON8, 108	815's K-P shorts
	090	815's K-P short
	Group 0	815 track 060
March 15	Group 8	5687 in 10 amp. GKP short
	All	Solder in socket PM7
March 20-22	Group 4	815 G_2K short, track IN4
March 23	Group N	815 short, tracks 15N, 17N
March 29	Group 4	815's K-filament leakage, tracks 124, 134

It was ovserved that most of the 815's replaced were surplus tubes; checking of all surplus 815's in the unit was begun.

The following circuit changes were made in the drum storage unit during the mongh:

1) Position and duration of the playback strobe pulse were reset. Positioning of the buffer gate pulse was reset.

2) A circuit was installed to hang up the Illiac whenever a non-existent track is consulted. The same circuit is used to maintain the dc input level to the playback amplifiers at approximately +80v whenever an address of a non-existent word appears in R_3.

Difficulty was encountered in production runs of the Drum Centroid Estimated Communalities code written by Kern Dickman of the Psychology Department. At the end of March, the trouble had been traced to effects of switching one grid selection bus (N23) over a long interval of time (50 words or more). It was observed that switching over a long period gives the effect of a low gain failure, particularly on track 234.

Attempts were made to correct the phase shift between drum track signals by simulating the added capacitance of the drum leads with lumped capacitances and also by installing shunt resistors across the head, either directly off the heads or on the other end of the drum cable. Although the phase shift could be changed in this manner it was found that the gain tolerance with the drum test code either decreased or showed no important changes. This is thought to be due to a change in the amplitude, frequency response, and signal shape when these modifications are attempted.

With no good method of regulating the phase shift problem tests were made to find what playback strobe pulse length and position with respect to record strobe produced the best gain tolerance. This was determined to be a P.S. length of 3 μs and position as shown below.

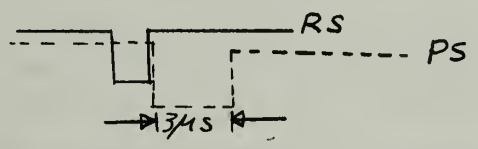


Figure 1

Measurements of the phase shift of each track were made and recorded in attempts to correlate track failures and phase shift. No definite conclusions were evident.

A new circuit was designed and installed which supplies a clamp dc voltage level for the inputs to the four main playback amplifiers when the address digits refer to a non-drum address. This circuit also supplies an inhibit signal for the drum coincidence which will hang up the machine if a drum order has an address in excess of 31LL sexadecimal.

High Speed Reperforator

The shop completed the high speed repreforator. All the circuits and operations were checked out and modifications made where required. The unit was found to operate at 30 characters per second rather than the anticipated 60

characters per second under normal settings of the punch A and B gates and the readers. This is because the time for the clutch on the reader to engage and move the tape to the next character is greater than the time between the B gate and A gate on the punch. Tests were made by readjusting the reader clutch and punch gates which allowed the unit to operate at 60 characters per second. These ran successfully, but since the tolerance on the reader voltages and on the correct operation of the punch were greatly reduced it was not thought advisable to use these settings for continued operation. The new readers being constructed show promise in increasing the unit's speed from some tests made with a new reader. The unit was installed for use in the Teletype Room.

VII. RESEARCH ON COMPUTER COMPONENTS. (This work is supported in part by the Office of Naval Research under Contract N6ori-07124.)

Transistor Test Computer

Work has been carried on in the following fields: transistor test computer circuitry, the delay-line application of the hole storage effect in germanium, the study of the dynamic behavior of a free-running racing register with 25 mμs operation time, the design of fast and, or and not circuits to go with the cross-coupled flip-flop and finally the behavior of a novel switching device.

An important modification was made on all the circuits and in the transistor test computer: it was decided to make all circuits behave as if the inputs were -2V when the inputs were floating. This will allow us to drive logical elements with bridge-modulator gates, these being originally designed to work into flipflops only. This simplifies certain parts of the control very considerably.

The core-memory circuits were completed and perfected in such a way that they can be run off the rather noisy supply busses, even in the presence of a special noise-generator. The memory was tested for several hours under these adverse conditions. Insufficient uniformity of the cores was overcome by using individual setting. A study program will be started to examine the feasibility of coincident current setting in our non-destructive read-out system.

The hole-storage delay-line memory was brought to a point where good and stable collector junctions can be produced at will. We are now examining the

effect of etching away the strained surface layers of the crystal: this will lower the surface recombination rate and therefore decrease the attenuation.

Logical circuitry to be associated with cross-coupled flipflops and using SB100 transistors is being developed. This offers some difficulties, since the emitter-base drop in these units is relatively high: the attenuation in an ordinary <u>and</u> circuit can become prohibitive. We have examined structures of the type given in Figure 2 below, making use of a GB-amplifier stage and an emitter-follower. The nominal swing is equal to that of the collector of the flipflop, i.e. from -0.5V to -4.5V.

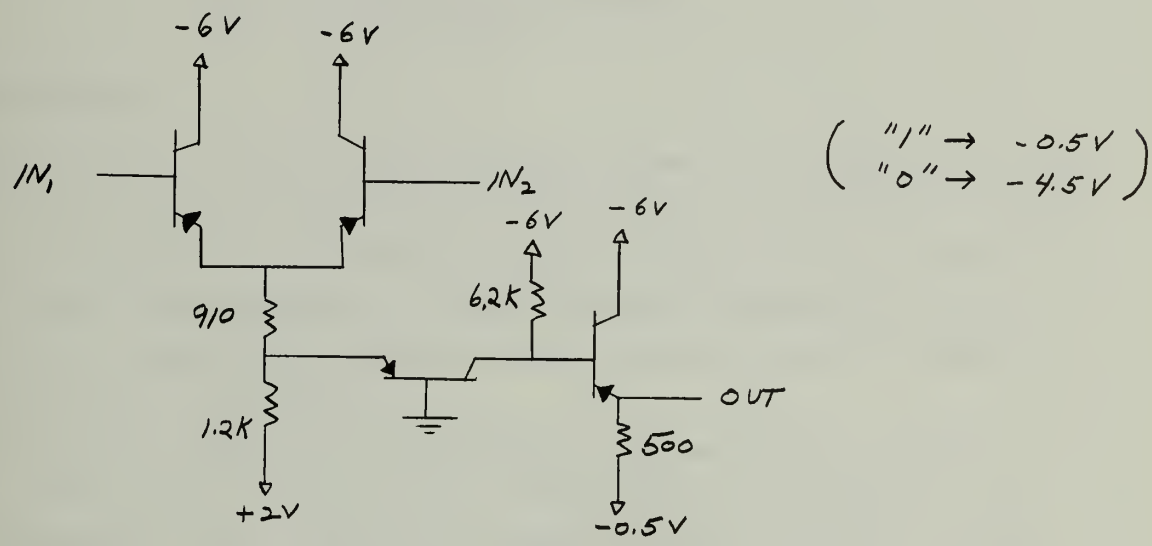


Figure 2

<u>SB-100 And Circuit</u>

In the course of searching for novel uses of semi-conductor devices the switching circuit of Figure 3 was examined. It uses a transistor in bilateral fashion: diodes from the emitter and load resistances. The voltage amplification of the circuit is given by the ratio of the backward to the forward resistance of the diodes. Depending on the applied voltages, either output 1 or output 2 furnishes an amplified signal.

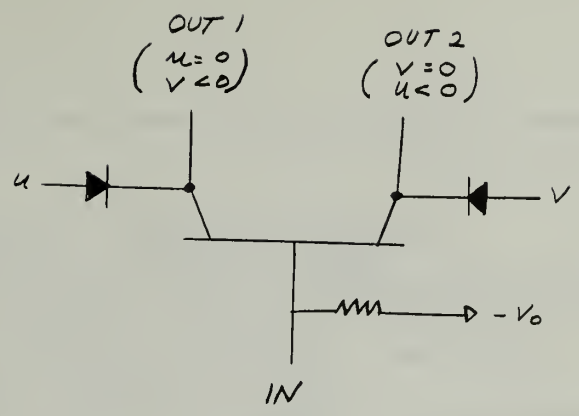


Figure 3

Bilateral Transistor Amplifier

VIII. CONSTRUCTION.

The main work of the shop for the month included the setting up of the memory test rack in the Electronics Room, the finishing of the construction of the 60 character per second reperforator unit, the construction of a new chassis (Dwg. 429) for the Illiac replacing one which had been damaged by oil from a condenser, and the construction of a frame for a Memotron tube to be added to the cathode ray tube output unit.

The 60 character per second reperforator has been placed in regular operation as noted earlier in this report. The Memotron to be added to the cathode ray tube output unit will enable observers to see an entire picture frame with all information retained unless a clearing push-button is actuated.

Additional repair work was carried out on a number of the photoelectric tap readers.

IX. REPORTS AND SEMINARS.

Seminars

"A Program for Composing Music with the Illiac" by L. M. Isaacson, March 6, 1956.

"Recent Computer Research at the National Bureau of Standards" by R. D. Elbourn, Data Processing Systems Division, National Bureau of Standards, March 13, 1956.

"A Program to Test Properties of Asynchronous Circuits" by W. Scott Bartky, March 20, 1956.

X. PERSONNEL.

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate
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Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
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DeWit, Roland, 1/2 time Res. Asst.
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Huffman, Wm. L., Computer Operator II
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Muller, David E., Res. Asst. Prof. of Applied Math.
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The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

R. E. Meagher

R. E. Meagher

REM/hc

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

April 1 - April 31, 1956

I. MATHEMATICAL RESEARCH AND PROGRAMMING. (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Theory of Speed-Independent Circuits

Work was begun on the design of practical speed-independent circuits, counters being designed using the kinds of logic in the Illiac and in the transistor test computer. The main purpose of this preliminary study is to find how much sacrifice in simplicity and speed will be required to yield a speed-independent computer.

Other interesting circuits which have been designed in an idealized way (i.e., no circuits have yet been built from these designs) are

(a) A speed-independent shift sequencing oscillator;

(b) A C-element (a flipflop having the functional equation $c = ab \vee c(a \vee b)$;

(c) A speed-independent "core" memory.

Additional work has been done in the study of weaker criteria for speed independence. The theory goes as follows:

(a) Define a relationship R between two states a and b of a finite asynchronous circuit, writing a R b if state b can follow state a with no intermediate states. Also let a R a for all a.

(b) Define a relationship a F b to mean either

(i) a R b or

(ii) a F c and c R B for some c.

(c) Define a relationship a E b to mean both a F b and b F a. We can show that the relationship a F b is transitive and that a E b is an equivalence relationship. If we let A and B be a pair of equivalence sets of states then if a is in A and b is in B and a F b we have a' F b' for every other pair of elements a' and b' in A and B respectively. Therefore we may write A F B. Between the sets of states the F relationship may be shown to define a partial ordering relationship.

The above results may not be new since they seem fundamental to the theory of linear graphs.

(d) Define a weaker form of speed independence as follows: A circuit is weakly speed independent with respect to an initial state s if for every a and b such that s F A and s F b there exists a c such that a F c and b F C.

(e) This definition may be shown to be equivalent to the statement that for the set S (containing s) there is exactly one maximum set M such that S F M. This means, of course, that if s is a member of a maximum set the circuit is speed independent.

(f) The stronger definition implies the weaker.

The importance of these results lies in the fact that this definition is the weakest that one can reasonably apply since denying it implies more than one final set of states. It is of interest, therefore, to see what types of circuits satisfy the weaker but not the stronger condition. The theory of the weaker type of speed independence is somewhat less interesting, however, since it is harder to test for, and because none of the present synthesis techniques apply.

Statistical Analysis

A program is in preparation for handling most analysis of variance problems. It computes least squares regression weights and other information necessary for the computing of various statistics. The problem of handling missing data will offer no difficulty.

One Error Checked Input

An input routine has been prepared for reading decimal numbers where each digit is represented by a 5-hole character with two holes punched rather than with straight binary coding of the digits. Data coded in this way will make possible checks both on data preparation and upon the tape reader. The preparation of data tapes will be relatively simple because most of the problems involving large volumes of data have the data on punched cards. The card to tape converter will simply be wired to furnish the proper conversion.

Sturm-Liouville Systems

A total of 32 production runs of Sturm-Liouville programs were completed for meshes of 9 and 13 points. Runs for 17 mesh points will also be carried out.

II. ANALYTICAL PROGRAM. (This work is supported in part by the National Science Foundation under Grant G-1221.)

The results obtained in the study involving an approximate procedure for dealing with the Einstein field equations have been written up in a paper entitled "Approximate Solutions of the Einstein Equations for Isentropic Motions of Plane Symmetric Distributions of Perfect Fluids," which will be submitted for publication. In this paper an approximate procedure is developed and applied to the problem of determining the gravitational and hydrodynamical fields associated with a plane-symmetric distribution of a perfect fluid with arbitrary caloric equation of state in isentropic motion. Special relativistic hydrodynamics in co-moving coordinates are discussed and methods are given for solving specific problems. These solutions provide a zero order approximation of the corresponding general relativistic problems. The linear equations describing the higher order corrections are discussed and the application of the method of characteristics is pointed out. The existence of shock waves in special relativity makes plausible their existence in general relativity, and they may be used to avoid using physically unacceptable solutions of the field equations.

III. PROGRAM LIBRARY.

The following four programs were added to the library in April:

J-2 (209) Roots of a Polynomial. Entire Program. This program computes the roots (real or complex) of a polynomial whose real or complex coefficients have been punched on tape. The method uses an iterative procedure of order 1.8. Results are printed in floating decimal form with 9 place roots and a 3 place residual obtained by substituting the root into the equation. The time for an nth degree polynomial depends partly upon the distribution of roots, but is about $18 + 5.2n + 0.08n^2$ seconds. The value of n may be quite large; polynomials of degree 100 have been solved.

XY-1 (210) Drum Clearing Decimal Order Input. 25 words. This routine differs in no way from Library Routine X-1 except that it is preceded by a drum clearing bootstrap to clear drum locations 2,560 to 12,799. The extra time required is 14 seconds.

S-4 (212) Exponential. 21 words. This program uses a continued fraction expansion to compute e^x. The maximum error is 5×10^{-12} and the maximum time required is 11.3 milliseconds. The program may be readily modified to exchange accuracy for time. For example, if only 4 figure accuracy is required, the time is reduced to 6.5 milliseconds.

M-18 (213) One-Step Automatic Eigenvalue-Eigenvector Program. This program is arranged so that the eigenvalues and eigenvectors of a symmetric matrix may be found merely by punching the scaled elements row by row. If the last element is followed by the character N, eigenvalues and eigenvectors are computed; if the character is a J, only the eigenvalues are computed. One additional character specifies the number of decimal digits to be printed. A number of checks are made during input and operation of the program. All eigenvalues and eigenvectors can be found for matrices up through order 23; if only eigenvelues are computed, the matrix may have an order as great as 40.

IV. MACHINE USE.

During April specifications were presented for 22 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 773. Numbers followed by T are for theses.

773 Computer. Statistics on 60,000 Digits of e. This program calculates χ^2 tests on the decimal expansion of e considered as a fraction in the scale of 10, of 100, and of 1000.

774 Computer. Multiple Precision Interpretive Routine. This was a special problem for Mathematics 385.

775 Psychiatry. Item Analysis by Successive Set Method. This is a factor analysis problem in which a 64-variable matrix is factored by the centroid method. The data for this problem came from the Temporal Lobe Project.

776 State Water Survey. Rainfall Measurement Error vs. Gage Density. This is a multiple correlation and regression analysis for the study of rainfall. It involves the mean rainfall of the sample area, the number of gages, the difference between the mean rainfall of the sample area and the best estimate of the mean from a dense network of gages, and the size of the area sampled.

777 Electrical Engineering. Electrical Engineering Problem. Library Routine J-1 is used to calculate the roots of a third-order polynomial where one coefficient is considered as a parameter and varied through 40 values. The problem is solved in connection with an electrical engineering course.

778 T Theoretical and Applied Mechanics. Symmetric Deformation of a Shallow Conical Shell. The computation is carried out using an iterative procedure to evaluate a non-linear integral equation, in which the first trial solution is an approximate one which requires the solution of a cubic equation.

779 Computer. Input a Sequence of Coded Fractions. This is an input routine in which each decimal digit is represented by a five-hole character with two holes punched rather than with straight binary coding of the digits. Data coded in this way will make it possible to have checks on data preparation and on the tape reader.

780 Electrical Engineering. Investigation of Stability of 3-Stage Feedback Amplifier. The problem is concerned with the calculation of the roots of a polynomial, and Library Routine J-1 is used.

781 T Management. Experience Rating in Unemployment Insurance. This problem is designed to study an experience rating system for unemployment insurance which might operate as a countercyclic agent by imposing high rates when business conditions are good and providing tax relief when business is bad.

782 Structural Research. Natural Frequencies of Skew Slabs. This is an exploratory study of the use of difference equations for the determination of the natural frequencies of skew slabs. The equations are of the form $A - \lambda B$, and Library Routine M-5 is used to calculate the eigenvectors.

783 Structural Research. Stresses in Skew Slabs. This is an exploratory study of the use of difference equations for the analysis of the state of stress in skew slabs. Library Routine L-2 is used to solve the equations.

784 Agricultural Economics. Variations in Monthly and Yearly Receipts at Illinois Grain Inspection Points. The problem requires computing variation coefficients with three series of variables, and Library Routine K-2 is used for the computation.

785 Institute of Communications Research. D Scores on Word Association. This is an analysis on data obtained from the University of Minnesota on about 100 stimulus words for word association. It is known what response is most likely to be given to a standard set of 100 stimulus words by a large population of people and each stimulus word produces several responses with significant frequencies. The statistical analysis carried out here is intended to test the hypothesis that the meaning similarities between stimulus and response words and word association are related.

786 German Department. Ratio of Text Length to Vocabulary Content. Frequency of distribution of words in German as compared to theoretical distribution according to harmonic series is being studied.

787 Southern Illinois University. This is a multiple curvilinear regression problem concerned with determining the best method of carrying out logging operations in forestry management.

788 Psychology. Prediction of Scholastic Achievement. This program is intended to test the hypothesis that configurations of factors in a battery of predictor tests will have a higher relationship with a criterion than will linear combinations of these factors. The work will be carried out with programs from the Illiac Library and the Psychology program library.

789 T Physical Education for Men. Analysis of Physique and Motor Skills in Children. Statistical analysis with library routines will be carried out to determine the primary factors involved in the growth of children and the relationships to certain motor skills. The results may help to determine the validity of Sheldon's three body type components and their applicability to children.

790 Electrical Engineering. Boundary Value Problem in Electromagnetic Wave Theory. The problem to be solved is a system of partial differential equations subject to certain boundary conditions arising in electromagnetic wave theory. The problem is approximated by using a grid method which leads to a system of simultaneous linear algebraic equations.

791 Computer. Factorization of Mersenne Type Numbers. This is an experimental routine on a new method for factoring numbers of the form $2^m - 1$.

792 University of California. Voting Behavior in San Francisco. Principal axes factor analysis will be performed to study the relationships among a group of sociological variables concerned with voting behavior in San Francisco.

793 Bureau of Educational Research. Analysis of School Administration Practices. Standard library routines will be used to calculate zero order and selected higher order partial product moment coefficients and to carry out a factor analysis on data which have been collected on school systems in Illinois using 8 school administration variables.

794 Department of Public Welfare. Prodromal Factors in Mental Illness. The main purpose of this research is to isolate factors which will be important in the personality patterns of children who have been seen by a school or community agency and a part of whom have later become mentally ill; to correlate these personality factors to those of mentally ill adults; isolate those factors common to both; to differentiate between those children who later become mentally ill and those who do not; to differentiate specific patterns of mental illness in the adult and their relationship to the childhood patterns.

Table I shows distribution of machine time for the month of April.

TABLE I

Regular Maintenance and Illiac Engineering	49:14
Unscheduled Maintenance	33:32
Drum Engineering	31:26
R.A.R.	8:35
Leapfrog	48:44
Wasted	:12
<u>Use by Departments</u>	
Computer Group	23:35
Physics	32:10
Control Systems Laboratory	46:01
Structural Research	24:40
Structural Research (AF 24994)	2:11
Structural Research (AF 170 Teapot)	:42
Psychology	11:33
Psychology (Navy Task 35)	2:55
Electrical Engineering	:14
Electrical Engineering (AF 3220)	:38
Chemistry	78:57
Agriculture	16:20
MURA	102:44
Inst. Comm. Res.	2:33
Southern Illinois University	5:25
University of California	:13
Iowa State University	2:38
Illinois Psychological Institute	1:36
Classes	12:18
Demonstrations	1:38
Miscellaneous	16:23
	557:07

V. ERROR FREQUENCY AND ANALYSIS.

The machine is normally used for "engineering" and maintenance between 8:00 A.M. and 12:00 N, and for a check of its performance between 6:00 and 6:30 P.M. of each weekday. Since the periods between 8:00 A.M. and noon, together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between noon and 8:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between noon and 8:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 6:00-6:30 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This overall system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instand of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for April.

TABLE III

Memory	2	Run-over of maint. period	1
Memory Synch. Chassis	1	Output	3
Input-output	0	Control	0
Input	5	Unknown	1
13 interruptions due to trouble which developed in March.			13

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
4/2/56	13:57	6:03	1	(1) V12-5687 in memory control broken	:00	:50	0
4/3/56	19:17	:43	1	(1) Light on Reader B burned out Interruption due to error reported in March	:00	1:21	0
4/4/56	19:54	:06	0	Interruption due to error reported in March	:00	:58	0
4/5/56	20:00	:00	0	3 interruptions due to error reported in March	:00	1:22	0
4/6/56	18:30	1:30	0	3 interruptions due to error reported in March	:00	3:26	0
4/9/56	12:35	7:25	1	(1) Screw came out of punch coupling #5 3 interruptions due to error reported in March	:00	1:08	0
4/10/56	14:32	5:28	1	(1) Possible reader K error 2 interruptions due to error reported in March	:00	1:36	0
4/11/56	19:42	:18	2	(1) Tape backed up in punch (2) Screw came out of punch connector	:00	1:06	0
4/12/56	20:00	:00	0		:00	:56	0
4/13/56	20:00	:00	0		:00	1:02	0
4/16/56	19:57	:00	0		:03	1:15	0
4/17/56	19:12	:43	1	(1) Mem. pos. 2^{-29} V8a shorted	:05	1:14	0
4/18/56	20:00	:00	0		:00	:47	0
4/19/56	19:27	:33	1	(1) Runover of morning maintenance	:00	:59	0
4/20/56	20:00	:00	0		:00	:49	0
4/23/56	19:45	:15	1	(1) Reader B bulb burned out	:00	1:07	0
4/24/56	18:24	1:36	1	(1) Replaced memory synch. chassis	:00	:42	0
4/25/56	17:40	2:18	2	(1) Leapfrog address in copy one incorrect by S1 but reason unknown	:02	2:02	2

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
				(2) Probably reader error			
4/26/56	20:00	:00	0		:00	:58	0
4/27/56	20:00	:00	0		:00	1:06	0
4/30/56	19:55	:05	1	(1) Bulb on Reader K out	:00	1:30	0
TOTALS	392:47	27:03	13		:10	26:14	2

VI. COMMENTS ON ILLIAC AND RELATED FACILITIES.

Auxiliary Drum Memory

During the month, the investigation of the errors occurring in the Drum Centroid Estimated Communalities program written by Kern Dickman was continued. It was found that a positive grid selection signal reduced the voltage on the switch tube and preamplifier tube (6AU6) plates to +5 volts, approximately. As a result, the 6AU6 was operating in the non-linear region of the plate characteristics and the screen current was no longer constant. The switch tube grid resistors are being increased from 10K to 47K; at the end of the month 88 of the 200 resistors had been changed.

By the end of April, 80 of the 95 surplus 815's had been checked. Sixty of these tubes failed to meet original specifications and were replaced. The number of 815 tube failures decreased as a result.

The air-cooled Freon condensing coil of the drum cooling unit was replaced by a water-cooled condensing coil. The amount of air flowing through the cooling and drum storage units was increased and baffles were installed to reduce the temperature of hot spots in the drum storage unit.

An error in wiring and drawings of the playback amplifiers was discovered. The screen voltages of the pentode amplifiers PA4 and PA7 were at 26v rather an 82v. After correction of the error, new gain curves were obtained for the amplifiers. The sensing levels for setting the "a" and "b" flipflops in the playback amplifiers were again equalized.

The positive voltage supplied to the drum circuits when the unit is disconnected from the Illiac were increased from 0v to +5v, in order to more closely approximate the actual voltages supplied by the Illiac. Recording on certain tracks was marginal or impossible when the drum unit was disconnected until this change was made.

Final corrections on all drum drawings are now in process.

Summaries of tube and component failures during the month are presented as Tables IV and V.

Beginning May 1 the drum will be considered a regular operating unit of Illiac and hence all failures or interruptions will be reported in the regular table.

TABLE IV - Tube Failures on Drum

Quantity	Type	Nature of Failure	Repair Time	Location
60	815	Mostly low emission; some k-Fil. leakage	Routine	PR chassis
1	6AU6	Sg - short	5 min.	PR chassis Track 260
1	815 (New)	K-Sg. (Flick-short)	25 min.	PR chassis Track 020
1	6AU6	K-fil. short	15 min.	V_2 in 01 PA
1	6AU6	K-Sg. short		V_7 in 01 PA
2	6J6	K-G_2, K-fil short		V_{10} and V_{13} in 01 PA
1	5687	Triode 1 - low emission	10 min.	MAb27
1	6BQ7	K-fil and G_2 (flick)		MAb39
1	2C51	K_2-G_2 (flick)	5 min.	CN_{32}
1	815 (New)	Intermittent broken filament	10 min.	PR chassis Track 250
1	815 (new)	Low emission, triode #2	30 min.	PR chassis Track 174
1	815	Low emission, triode #2		PR chassis Track 26N
1	6J6	Broken envelope	20 min.	RC19

(73 vacuum tubes replaced during month of April)

TABLE V - Component Failure on Drum other than Tubes

Date	Component and/or type of failure	Repair Time	Comment
4/2/56	Fuse, +150v DC	30 min.	Fuse blown due to short in jumper cable installed for Illiac test equipment.
4/2/56	Bad solder joint in +150v DC section of filter panel.		This was located when DC failed to hold after above fuse replaced.

TABLE V (Continued)

Date	Component and/or type of failure	Repair time	Comment
4/23/56	Replaced AC elapsed time meter	45 min.	Worn gear slipped on shaft and screwed itself from under meshing toothed gear.
4/30/56	Three filament voltmeters not reacting to changes in variac positions. Meters are probably mechanically defective. Not replaced to date.	60 min.	Voltage varied correctly at meter connections. Set variacs w/test meter, and tabled repair and testing for time being.

TABLE VI - Frequency of Tube Replacement in Drum by Type

Quantity	Tube Type
61	815 (war surplus)
3	815 (new)
3	6AU6
2	6J6
1	6BQ7
1	5687
1	2C51

Memory Test Rack

A number of changes and improvements have been made in the Williams tube test rack which had been originally constructed some time ago. These changes make the test rack operate more exactly like memory circuits now used in Illiac, to make it easier to compare the operation of memory chassis or tubes.

VII. RESEARCH ON COMPUTER COMPONENTS. (This work is supported in part by the Office of Naval Research under Contract N6ori-07124.)

Transistor Circuits

All plug-in units for the transistor test computer have been constructed and all chassis are wired, with the exception of decoding and control. The logical oscillator, the sequence counter and the order counter as well as the adder and the A-register (with R^3) have run simultaneously and have passed the initial tests. Some minor modifications were made to insure rise-times of the order of 1 μs throughout the machine. Presently the memory circuits are under test. A small dual-trace monitor scope has been built for the transistor test computer.

The set of logical circuits adapted to the cross-coupled flipflop has been extended to include or and not circuits. Both these circuits have a sum of delay and rise-time of about 40 mμs. An adder using these circuits is being designed. The layout of the two new circuits is given in Figures 1 and 2.

The or circuit uses two emitter-followers T_1 and T_2 to drive two GB-amplifiers T_3 and T_4. The common collector is kept out of saturation by transistor T_5 while the output is obtained from another emitter-follower T_6. This rather elaborate arrangement is necessary if high speed of operation is desired; if npn transistors in the 50 mc range were available, great simplifications could be introduced.

The not circuit too is rather lavish in its use of active elements and for precisely the same reasons as those quoted above. Here an emitter-follower feeds an inverter, the collector of which is clamped to eliminate saturation. The output is obtained from another emitter-follower. It should be remarked that since these circuits were designed, diodes have been available which work as clamps at the desired frequencies: This eliminates one active element in each one of the preceding circuits.

Static tests were performed on a new flipflop circuit shown in Figure 3. This circuit uses a pnp-npn combination (instead of the point-contact units) in an MIT-configuration. The MIT-flipflop is based on the negative input impedance of junction units: looking into A and B one obtains a typical "N"-characteristic. It turns out that non-saturation is not difficult to attain

(All transistors are of the Type SB 100)

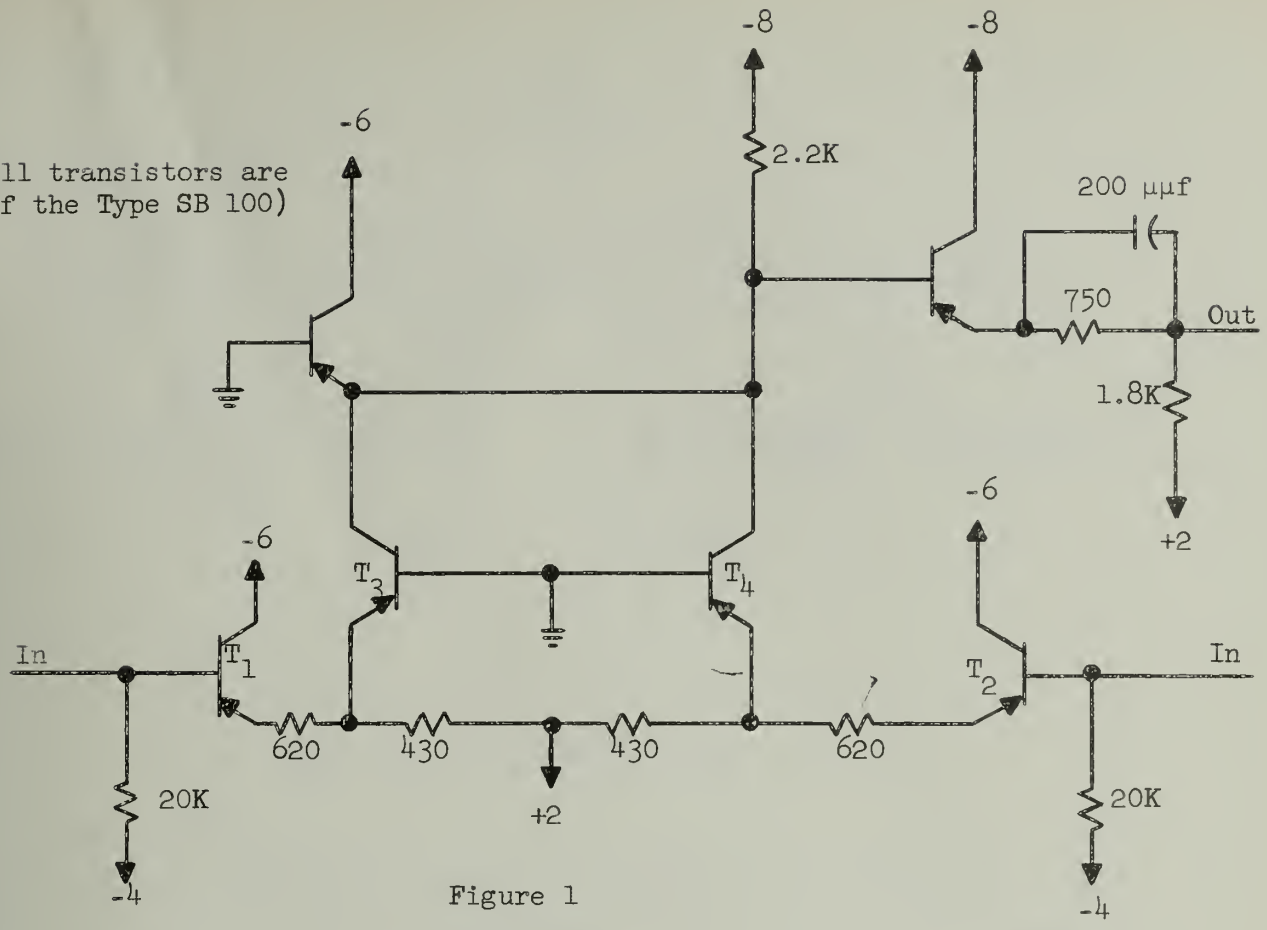
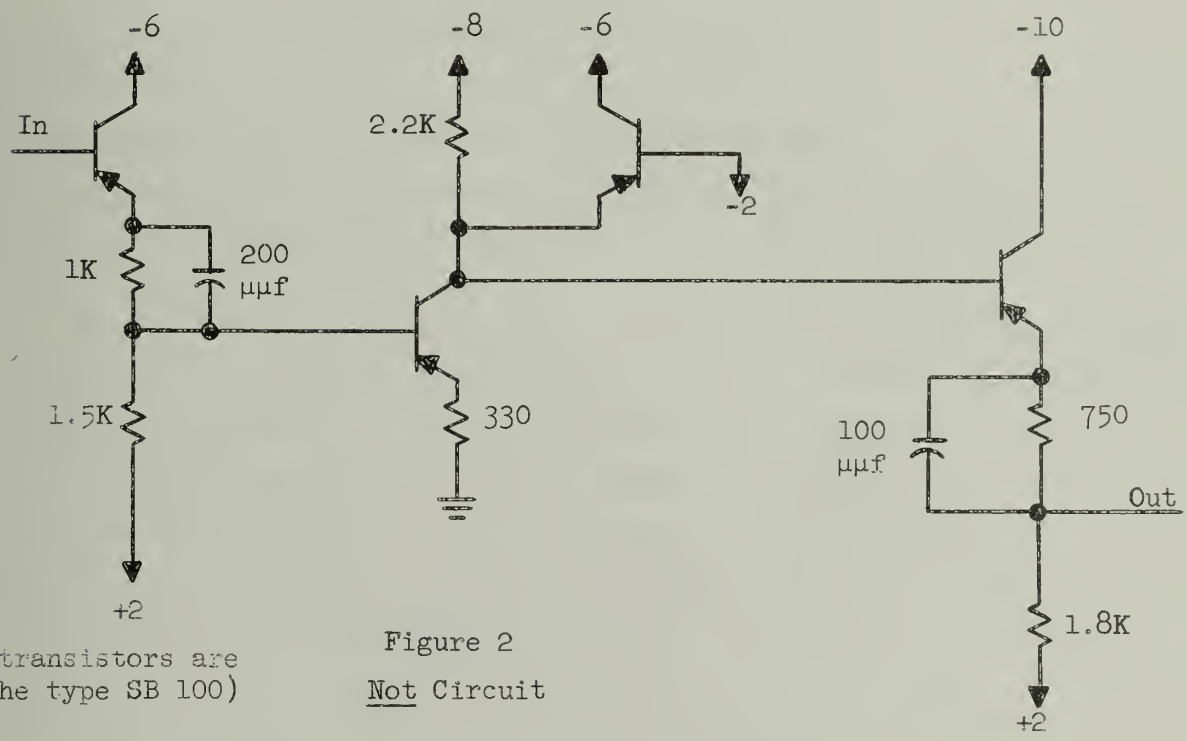


Figure 1

Or Circuit



(All transistors are of the type SB 100)

Figure 2

Not Circuit

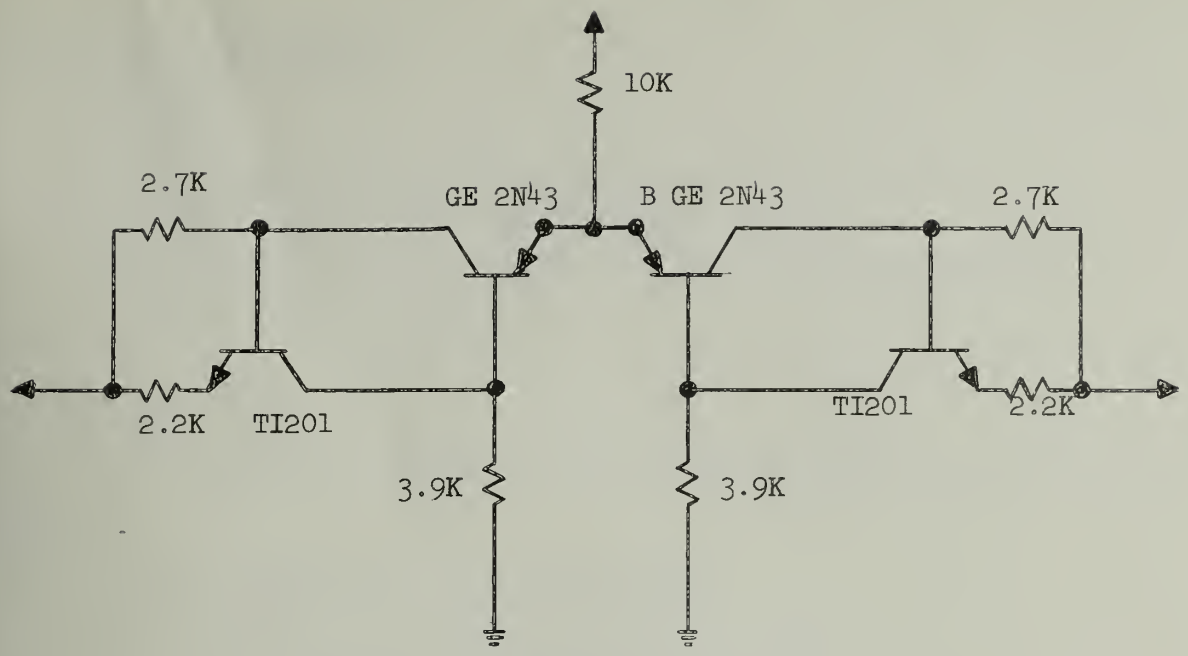


Figure 3 - MIT Hook Flipflop

with the new design and that tolerance conditions can be met easily. Also the circuit requires only one base delay-time in order to "hold"; tests on the operation time will be made soon. It seems possible to reduce the number of components.

VIII. CONSTRUCTION.

The construction of the circuits to operate a Memotron cathode ray tube in conjunction with the ordinary cathode ray tube output from Illiac has been finished. A second portable power supply of ±30v for transistor circuits was assembled.

The design of the frame for a more permanent high-speed tape reperforator and a more permanent high-speed tape comparing unit was finished. These units, when constructed, will take the place of the temporary arrangements which are now in use in the Teletype Room. A logical change in the high-speed reperforator (adding a buffer register) will permit it to operate at 60 characters per second as compared with the presently available 30 characters per second unit.

An inventory and card numbering system has been devised for the stock room.

IX. REPORTS AND SEMINARS.

Seminars

"A Program to Test Properties of Asynchronous Circuits" Part III, by W. Scott Bartky, April 10, 1956.

"The Ferranti Pegasus Computer," by Dr. Donald W. Gillies, April 17 and 24, 1956.

X. PERSONNEL.

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate
Bartky, W. Scott, 1/2 time Res. Asst.
Black, Billie G., Draftsman (started 4-30-56)
Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
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Student Assistants

Chan, Saifook (started April 16)
Dean, Floyd R.
Geis, John P.
Goodman, Robert
Kirwan, John F.
Ogata, Albert I.

The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, D. G. Gillies, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

R. E. Meagher

R. E. Meagher

REM/hc

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

May 1 - May 31, 1956

I. MATHEMATICAL RESEARCH AND PROGRAMMING. (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Theory of Speed-Independent Circuits

Most of the time during May was in writing up previously obtained results.

Analysis of Variance

A program was completed for handling the general model of the analysis of variance and covariance. The data are treated as integers from which the program computes the matrix of sums of squares and cross products, inverts it, and prints the inverse and the accounted for sum of squares and cross products.

Sturm-Liouville Systems

Calculations of the kth eigenvalue λ_k of $y'' + \lambda y = 0$ with $y(0) = y(1) = 0$ have been made using polynomial arcs of degree m for the approximations over an interval divided into 10 equal sub-intervals. The percent relative errors in the eigenvalues are given in the following table for $k = 1, 2, 3, 4, 5$ and $m = 2, 3, 4, 5, 6, 7, 8$

m \ k	1	2	3	4	5
2	.018	.308	1.249	4.192	7.498
3	.001	.052	.625	2.224	7.299
4	.000	.015	.022	.323	1.945
5	.000	.000	.019	.104	.767
6	.000	.000	.003	.106	.383
7	.000	.000	.000	.028	.723
8	.000	.000	.000	.004	.203

Similar results were obtained with the interval divided into 14 and 18 parts. A paper describing the results was prepared.

Analysis of Digits of e

A program is being prepared to do a statistical analysis on the 60,000 decimal digits of e which were calculated several years ago.

One analysis was done, but it is felt that a more complete one is desirable.

Input-Output Programs

A new version of the Decimal Order Input routine (Library Routine X-1) has been prepared and will be used in the future. The new routine was originally $3\frac{1}{2}$ words shorter than the old one and these $3\frac{1}{2}$ words are now used as follows:

a. $1\frac{1}{2}$ words to make the two entries to the routine at words 999 and 1014 compatible with the old version,

b. 1 word to speed up the read-in loop,

c. 1 word to free location 2 and allow an additional parameter by reducing the temporary storage needs to locations 0 and 1 only.

A new print routine will be placed on the magnetic drum so that it can be used in connection with all programs needing a print routine for either integers or fractions and thus reduce the space needed for print routines. The new routine has a number of advantages over all of the others in the library.

a. It handles up to 12 digit fractions.

b. The round-off is nearly exact on fractions.

c. There are 3 ways of representing the sign of a number.

d. It prints a decimal point.

e. It prints the sign immediately before the number (not leaving spaces as in some zero suppression programs).

f. It does not print spaces after the number.

A new input routine handles integers or fractions, depending upon entry, and is shorter and faster than the previous N-2 which handles only fractions.

Use of Magnetic Drum

One of the principal reasons for interest in new input-output routines is the desire to use the magnetic drum storage most effectively. At present 2,560 words of the 12,800 on the drum have been set aside for the storage of engineering programs and library routines. The new Decimal Order Input will be placed on the drum and the initial starting instruction changed to a drum playback instruction for placing the Decimal Order Input or a bootstrap input routine in the Williams memory. After June 15th, it will no longer be necessary to have an input routine on the tape, although its presence on the tape will have no adverse effect. The next step is to make the Floating Address Program and the playback program for library routines (Routine Y-2) ready for drum use. It will then be possible to store the most-used library routines on the drum. It is expected that this will be completed before the end of the summer.

II. ANALYTICAL PROGRAM. (This work is supported by National Science Foundation Grant G-1221.)

A paper entitled "On the Numerical Solution of Sturm-Liouville Differential Equations" by C. C. Farrington, R. T. Gregory, and A. H. Taub was prepared and will be submitted to a technical journal for publication. In this paper the well-known relation that exists between a Sturm-Liouville differential equation together with its boundary conditions and normalization condition and a problem in the calculus of variations is used to obtain approximations to the characteristic values and functions of the Sturm-Liouville equations. Two methods for exploiting this relation are described in detail. The methods were applied to the example

$$\frac{d^2y}{dx^2} + \lambda y = 0$$

with the boundary conditions

$$y(0) = y(1) = 0$$

and the normalization condition

$$\int_0^1 y^2 \, dx = 1$$

The characteristic values and characteristic functions obtained showed very good agreement with the exact solution to this problem. The detailed results are discussed on Page 1 of this report. In order to apply the methods proposed in this paper to more complicated Sturm-Liouville problems it will be necessary to devise a test for the accuracy of the results obtained applicable to problems for which the solution is not known. Various such tests are under investigation.

III. PROGRAM LIBRARY

The following two programs were added to the library in May. Program X-11 was prepared by Professor W. C. Jacob of the Department of Agronomy.

X-11 (208) Data Tape Checking for Library Routines K-2 and K-9. Complete Program. This is a program of the auxiliary library which aids in the preparation of data used in calculating product moment correlations and other statistical quantities. It counts quantities on the tape and compares with the specification provided by the user.

K-12 (211) Multiple Regression Analysis. Complete Program. This program makes use of the magnetic drum to do a multiple regression analysis for a number of variables not greater than 22. The number of observations is unlimited. The program is provided with various checks to catch errors that may arise in the data tape, the program tape, or in drum transfers. Speed depends upon a number of things, but, as an example, if there are 20 variables and 100 observations each given to 8 decimal digits then it will take about 7 minutes to read the program and observations,

print the correlations and covariance matrix, invert the correlation matrix, and print the standardized and unstandardized regression weights and their standard error, all printing to 8 decimal places.

IV. MACHINE USE

During May specifications were present for 14 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 795. Numbers followed by T are for theses.

795 Psychology. Serial Correlation in Detection Thresholds. Library Routine K-5 will be used to compute intra-session serial correlations on brightness detection thresholds gathered in 243 man-day sessions of simulated watch-keeping.

796 Illinois State Geological Survey. Fluid Saturation Distribution in Network Models of Porous Media. The overall problem is concerned with the study of fluid saturation distributions as they occur within the microscopic pore spaces of an oil reservoir. A mathematical model utilizing a network of capillary tubes will be used for the study.

797 Computer. Analysis of Variance. This program considers the general case of the analysis of variance problem. The program is essentially concerned with determining least squares constants.

798 Marketing. Variability in Consumption Expenditures. Library routines will be used to carry out a product-moment study on data which have been gathered from 155 families over 20 family expenditure variables.

799T Physics. Energy Spectrum of Electrons and Positrons in the Forward Cone. The Illiac will be used to perform integrations of various cross-sections over the bremsstrahlung spectrum.

800 Computer. Ladder Network Synthesis. The program carries out a partial fraction expansion of a quotient of two polynomials to produce a ladder network when this is possible. If it is not possible, the function is reduced to a non-realizable function and this function is printed.

801T Chemistry. Calculation of Spectral Energy Levels. The problem is a numerical solution of a cubic secular equation arising in the determination of a set of spectral energy levels.

802 MURA. Equations of Motion. Library Routine F-1 will be used for solution of the equations of motion of a particle when the values of the potential between the pole faces of electro magnets in a high energy accelerator are given.

803 Metallurgy. Study of Diffusionless Transformations. The Illiac will be used for the solution of a number of quadratic equations containing coefficients which have to be computed.

804 Dairy Science. Prediction of Milk and Fat Production. This is a statistical analysis using Library Routine K-2 to compute sums of squares and cross products from data involving breeding, herd and year. This analysis will be used to compute a multiple regression.

805 Psychology. D-Score Analysis. This is an analysis with a D statistic in which there are 8 scales per individual and 486 individuals in the sample.

806 Bureau of Economics and Business Research. Retail Sales in Local Areas. Library Routine K-12 will be used to compute multiple correlation coefficients and regression weights from data on retail sales volume figures for 51 towns in Illinois.

807 Computer. Drum Storage of Engineering Routines. This is a program which will place on the magnetic drum the important engineering routines which are needed for use with the Illiac.

808T Psychology. Similarity Study. The D statistic is being used in a study of the similarity of a person's description of himself and the description of several other persons.

Table I shows distribution of machine time for the month of May.

TABLE I

Regular Maintenance and Illiac Engineering	52:24
Unscheduled Maintenance	12:52
Drum Engineering	37:11
R.A.R.	7:10
Leapfrog	50:26
Wasted	:29

Use by Departments

Computer Group	24:33
Physics	26:46
Control Systems Laboratory	54:09
Structural Research	3:18
Structural Research (AF 24994)	3:25
Psychology	10:39
Psychology (Navy Task 35)	:15
Psychology (M.D. 569)	1:17
Electrical Engineering	9:02
Electrical Engineering (AF 62)	7:54
Electrical Engineering (AF 3220)	:36
Dairy Science (9B-2B)	2:26
Chemistry	47:17
Agriculture	8:28
MURA	175:41
Institute of Communications Research	1:17
University of California	:10
Southern Illinois University	4:47
Classes	26:00
Demonstrations	2:22
Miscellaneous	16:54
Total	587:48

V. ERROR FREQUENCY AND ANALYSIS

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for May.

TABLE III

Reader Errors	4
Punch Errors	1
Drum Errors	2
Scope Errors	1
	8

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
5/1/56	20:00	:00	0		:00	:53	0
5/2/56	19:58	:00	0		:02	:58	0
5/3/56	19:59	:01	1	(1) Film does not advance on scope.	:00	1:01	0
5/4/56	19:59	:01	1	(1) Reader "J" not reading correctly.	:00	1:36	0
5/7/56	20:00	:00	0		:00	:51	0
5/8/56	19:59	:00	0		:01	:44	0
5/9/56	19:49	:11	2	(1) Drum error. (2) Light on Reader "K" out.	:00	:39	0
5/10/56	19:52	:08	1	(1) Punch #5 failing.	:00	1:25	0
5/11/56	19:59	:01	1	(1) Leapfrog reader error.	:00	:57	1
5/14/56	20:00	:00	0		:00	:43	0
5/15/56	20:00	:00	0		:00	1:17	0
5/16/56	20:00	:00	0		:00	1:14	0
5/17/56	19:55	:00	0		:05	1:24	0
5/18/56	19:59	:01	1	(1) Drum error.	:00	:55	0
5/21/56	19:57	:00	0		:03	1:06	0
5/22/56	20:00	:00	0		:00	1:48	0
5/23/56	20:00	:00	0		:00	:56	0
5/24/56	20:00	:00	0		:00	:40	0
5/25/56	19:52	:08	1	(1) Bulb on Reader "B" out.	:00	:39	0
5/28/56	20:00	:00	0		:00	:59	0
5/29/56	20:00	:00	0		:00	1:29	0
5/31/56	20:00	:00	0		:00	:51	0
TOTALS	439:18	:31	12		:11	23:05	1

VI. COMMENTS ON ILLIAC AND RELATED FACILITIES

Auxiliary Drum Memory

Consideration is being given to allocation of the permanent drum storage space (locations 0-2599 inclusive). In particular, approximately 900 words, beginning at drum location 32, have been tentatively set aside for commonly used engineering routines. At the end of the month, the collection of routines associated with the leapfrog were modified in such a way as to be compatible with the Fishel-Gillies-Muller drum input routine and in such a way that both the ordinary leapfrog and the flying leapfrog are available.

During this month the process of changing all grid resistors of the pre-amplifier switch tubes from 10KΩ to 47KΩ was completed. Errors, of the type occurring in the Drum Centroid Estimated Communalities program last month are no longer a problem.

All of the surplus 815 record tubes have been checked. Of the remaining 15, 12 were discarded. Errors caused by grid-cathode or cathode filament leakage of 815's did not occur at all this month.

Additional baffles were installed in the input and exhaust systems of the air-conditioning system. The air flow was further increased. Temperature checks show that previous "hot-spots" are now well within tolerable limits. A "Fenwal" thermoswitch was installed for protection from high temperatures.

VI. RESEARCH ON COMPUTER COMPONENTS (This work is supported in part by the Office of Naval Research under Contract N6ori-07124.)

Transistor Test Computer

The transistor test computer has reached a stage where the tests of the over-all design could begin. To simplify the task, memory and registers (except R_3) were disconnected and the operation of logical oscillator, sequence counter, order counter, decoding, control and gate-drivers was checked. After some minor modifications (introduction of a certain number of level-restorers in particular) and the elimination of some marginal active elements, it was possible to go manually--by inhibiting the return-signals to the logical oscillator--through addition, subtraction, multiplication (preceded by a $A \rightarrow Q$ shift) and division (followed by a $Q \rightarrow A$ shift). It also proved

possible to cycle automatically through 4 subtract orders; it was verified that the rise-times under these conditions were still of the order of 1 μs. The total time for one cycle, consisting of: clearing the number register, setting the sequencing counter to zero, advancing the order counter, bringing the subtrahend to the number register, forming the difference in $\overline{A}$ and gating the result to A (each operation being checked by reply-back signals) is of the order of 100 μs.

The signal-to-noise ratio in the memory was considerably improved by introducing a pulse-sharpening stage between the selection matrix for the orders and the core drivers. Furthermore some critical voltages for the read-out amplifiers are now furnished by very low impedance filter networks. Tests seem to indicate that the memory is ready to be tied in with the rest of the equipment. It is hoped that another two weeks will be sufficient to complete this 735-transistor, 500-diode computer model. A complete report with schematics will be available soon.

Fast Transistor Circuits

A program has been started to investigate the possibility of very fast read-out (1 μs) core memories. In particular a non-destructive read-out system using two test-pulses of opposite polarity and giving a "have read" signal is under investigation. Multiple coincidence wiring is also being studied.

The speed of a half-adder stage using the fast set of logical circuits described in the last two issues of the technical progress report and the cross-coupled flipflop has been tested; Figure 1 shows the set-up: one

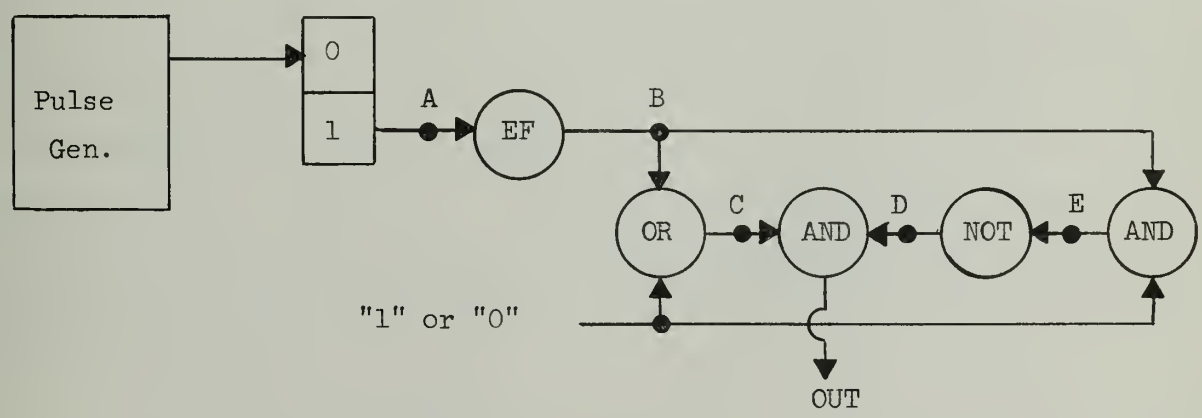

Figure 1

Rise-Time Test Set-up for a Half-Adder

input to the adder is held at a fixed level ("0" or "1"), while the other one is connected--via an emitter-follower--to the last moving point of a cross-coupled flipflop which in turn is driven by a pulser. Rise and fall times of the order of 50 mμs were attained with the circuit in all of its points ABCDE and OUT.

An "exclusive or" circuit of rather novel design was also tried out (see Figure 2). Although no carry is available in the present form, it seems to

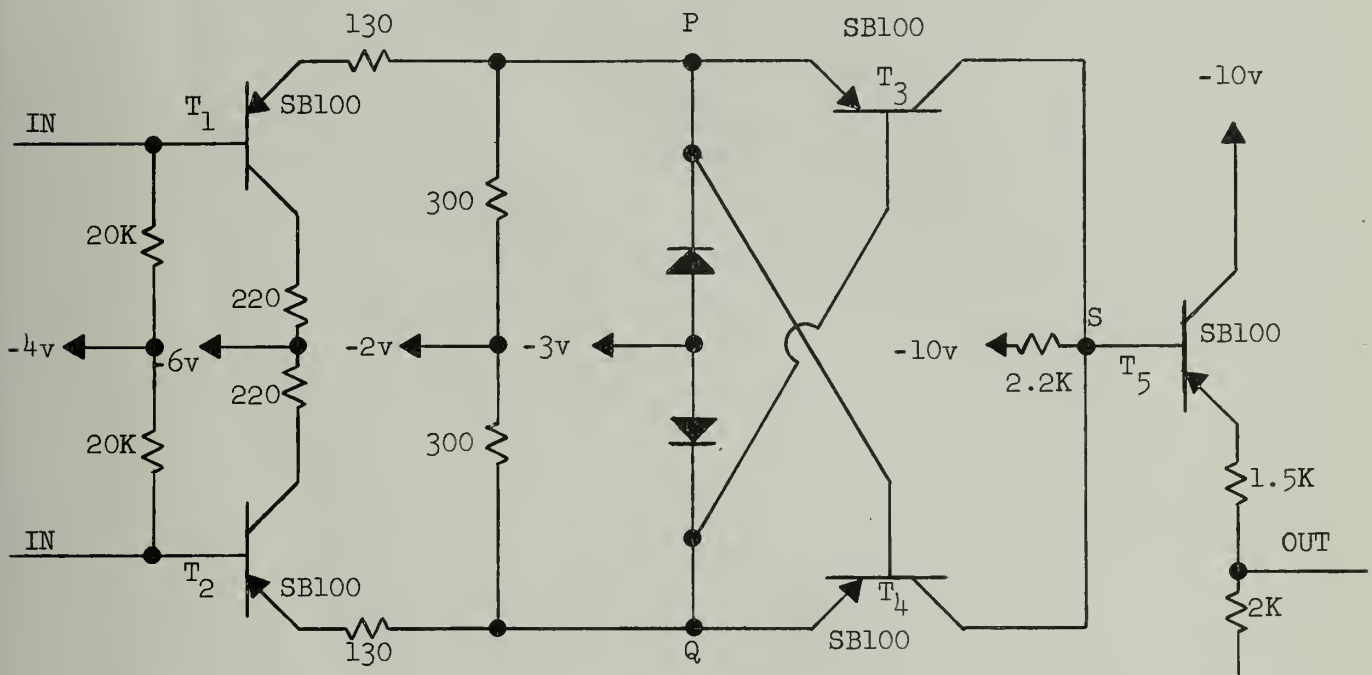

Figure 2

Exclusive Or Circuit Using Cross-coupling

be quite promising if certain tolerance problems can be solved. The principle of the circuit is as follows: Two transistors T_3 and T_4 have emitter-base cross-coupling (like the cross-coupled flipflop) and work into a common collector resistance. As long as the voltages at P and Q are equal--either at the "0" or at the "1" level--neither one of the units conducts. As soon as a difference in potential appears, one or the other transistor conducts and the potential in S goes up. T_1 and T_2 are input emitter-followers while T_5 is an output emitter-follower. With the above design used instead of the OR-AND-NOT-AND combination of Figure 1 rise and fall times of about 50 mμs were again attained.

Hook Flipflop Analysis

A preliminary analysis of the "MIT-Hook-Flipflop" described in last month's technical progress report has shown that no particular tolerance or design difficulties are encountered. Figure 3 gives the notation used in the summary of some calculations below.

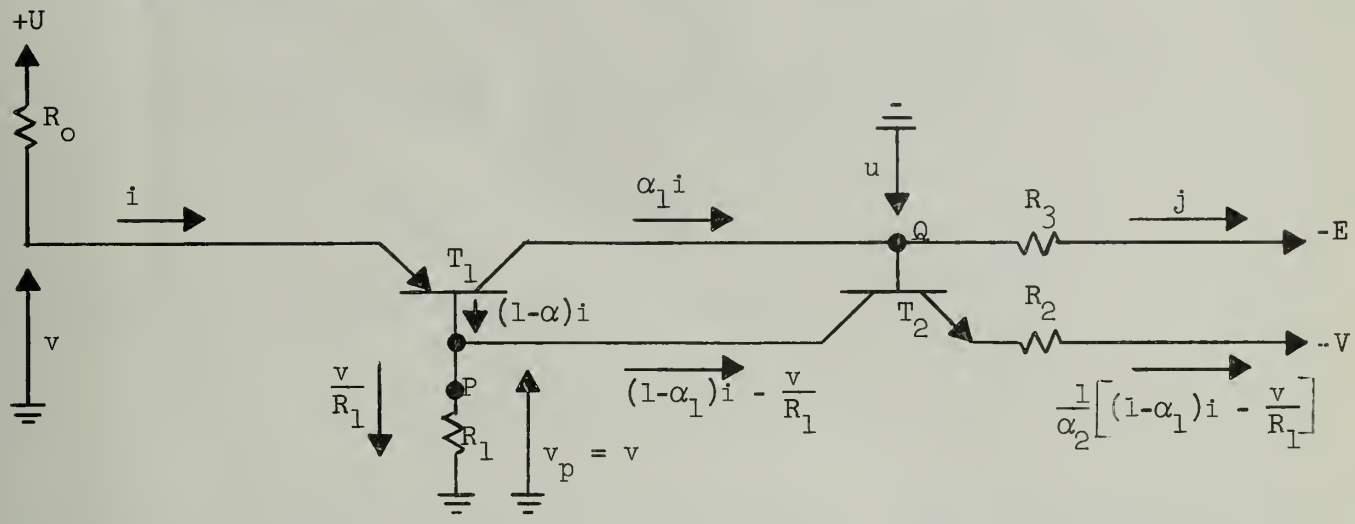

Figure 3

Voltages and Currents in One Half of a Hook-Flipflop

Note that for generality's sake R_2 and R_3 are returned to two different voltages. The currents and voltages refer to the condition where both T_1 and T_2 are on; the other side of the flipflop is supposed to be in the "off" state. Emitter base drops are neglected in the conducting transistors.

Introducing

$$i_o = \frac{E - V}{R_3}, \qquad \lambda = \frac{R_2}{\alpha_2 R_3}, \qquad \mu = \frac{1 - \alpha_2}{\alpha_2}$$

$$A = \alpha_1 - (\lambda + \mu)(1 - \alpha_1), \qquad B = -(\lambda + \mu)$$

one can easily see that

$$Ai = \frac{B}{R_1} v + i_o$$

meaning that the absolute value R_n of the negative resistance looking into the device from the left is given by

$$R_n = -\frac{A}{B} R_1 = R_1 \frac{\alpha_1 - (1 - \alpha_1)\left(\frac{R_2}{\alpha_2 R_3} + \frac{1 - \alpha_2}{\alpha_2}\right)}{\frac{R_2}{\alpha_2 R_3} + \frac{1 - \alpha_2}{\alpha_2}} .$$

In the case of high α-values this gives approximately

$$R_n \sim \frac{R_1 R_3}{R_2} .$$

Calling v_o the value of v when i = 0, we obtain

$$v_o = \frac{R_1 i_o}{\lambda + \mu} = (E - V) \frac{R_1}{R_2} ,$$

meaning that the negative-resistance characteristic starts at the origin when E and V are made equal. Figure 4 however shows the general case. In this figure we actually draw the combined characteristics of the two halves of the

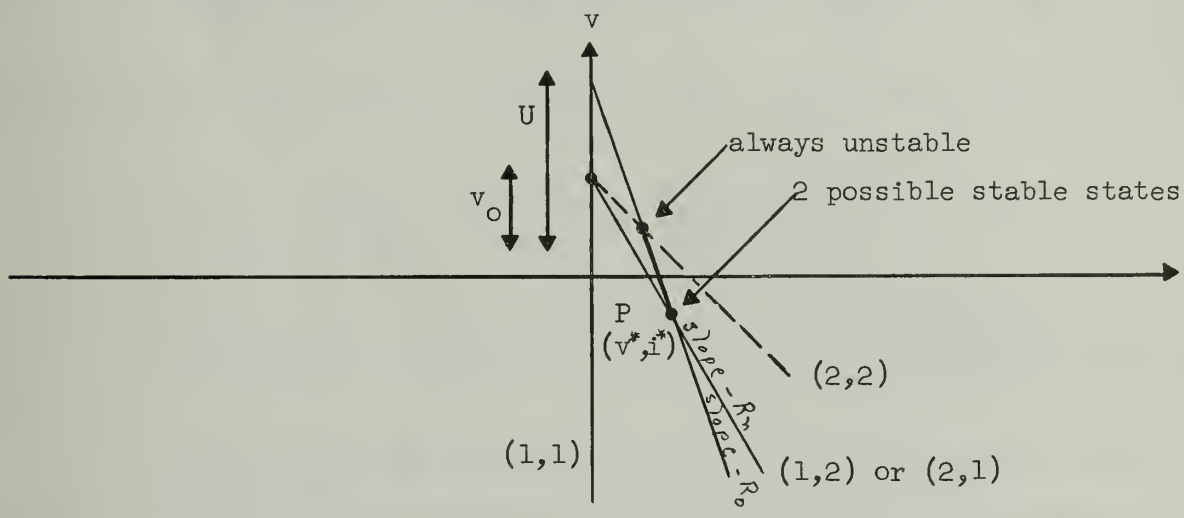

Figure 4

Operational Graph of a Hook-Flipflop

circuit: "1" means cut-off, "2" means in the active region. No saturation region "3" is considered because the non-saturation condition below is supposed to be respected. In the case of symmetric halves we then have three segments (1,1), (1,2) = (2,1) and (2,2) all meeting in point $(0,v_o)$. The possible states are determined by the intersection of the load line (through 0, V, having slope $-R_o$) with the characteristics. It turns out that only point P--intersection of the load-line with (1,2) = (2.1)--can be stable. The voltage and current in the "on" half are then

$$i^* = \frac{V - v_o}{R_o - R_n}$$

$$v^* = \frac{R_o v_o - R_n V}{R_o - R_n}$$

The non-saturation condition for both transistors simultaneously is $v_p(=v) > u$, i.e.

$$\frac{R_1 v_o - R_n U}{R_o - R_n} > - V + \frac{R_2}{\alpha_2} \left[(1 - \alpha_1) i^* - \frac{v^*}{R_1}\right].$$

In the case E = V (giving $v_o = 0$) and $\alpha_1 = \alpha_2 = 1$ this reduces to

$$\frac{V}{U} > \frac{R_n}{R_o - R_n} \cdot \frac{R_1 + R_2}{R_1} = \frac{R_2 R_3 + R_1 R_3}{R_o R_2 - R_1 R_3} .$$

Given the set $R_o \ldots R_3$, u it is therefore always possible to find a V such that there is no danger of saturation. No diodes are necessary to achieve this effect.

A racing register with GE 2N43 and TI202 (i.e. 1 mc) transistors using difference amplifier gates coming out of Q and going into P has shown operation times of 1.3 μs as compared to 1 μs obtainable with a cross-coupled flipflop using the same transistors. It seems possible to attain the same speed after some refinements have been made.

Beam Deflection Tubes

In an effort to examine the fastest possible computer circuits, consideration was given some time ago to beam deflection tubes. The tests made at that time using existing commercial tubes was reported in the Technical Progress Report of October 1955. The requirements for beam deflection tubes for digital circuits were discussed with engineers of the Tube Department of the Zenith Radio Corporation. This corporation then made up four special tubes and they have been tested in circuits here. These tubes have the particular advantage that the deflection electrodes operate at the same potential as the collectors. Thus the flipflop circuit does not need a dc potential transfer network of the kind indicated in the October 1955 report. The circuits are then relatively simpler.

The Zenith tubes have been tested in a racing register using these very simple flipflops. The operation time of the circuit was 75 millimicroseconds.

VII. CONSTRUCTION

A new transistor power supply consisting of 10 storage batteries and an associated charging system was completed. A number of repairs were made to high-speed tape readers. Work was carried out to equalize the distribution of cooling air in the drum unit. This required the addition of baffles and a somewhat increased flow of air in the main drum frame.

The main work of the shop during the month has been devoted to a final design and construction of a photoelectric tape comparer and a high-speed reperforator for operation at 60 characters per second. Both of these units are similar to the temporary units now in the Teletype Room, but both will contain a number of improvements. The main frame for the photoelectric tape comparer unit has been partly built.

IX. PERSONNEL

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate
Bartky, W. Scott, 1/2 time Research Assistant

Black, Billie G., Draftsman
Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
Clements, Virgil F., Jr. Laboratory Mechanic
DeWit, Roland, 1/2 time Res. Asst.
Ehmen, Mrs. M. Gwendolyn, Computer Teletype Operator
Farrington, Carl C., 1/2 time Res. Asst.
Fishel, Jerome H., 1/2 time Res. Asst.
Gillies, Donald D., Res. Asst. Prof. of Appl. Math.
Goldberg, Jack L., 1/2 time Res. Asst.
Golub, Gene H., 1/2 time Res. Asst.
Hill, Robert S., Computer Operator I
Holm, Walter H., Jr. Electronics Tech.
Huffman, Wm. L., Computer Operator II
Kerkering, Thomas E., Sr. Laboratory Mechanic
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Lytle, Harold R., Jr. Electronics Tech.
Meagher, R. E., Chief Engineer
Metze, Gernot A., 1/4 time Res. Asst.
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Miller, Raymond E., 1/2 time Res. Asst.
Muller, David E., Res. Asst. Prof. of Applied Math.
Nash, J. P., Res. Prof. of Appl. Math.
Nelson, James C., 1/2 time Res. Asst.
Newmark, N. M., Chairman, Executive Committee
Pelg, Edmund, Jr. Electronics Technician
Peterson, Donald A., 1/2 time Res. Asst.
Poppelbaum, W. J., Res. Asst. Prof.
Ray, Sylvian R., 1/2 time Res. Asst.
Robertson, James E., Res. Asst. Prof. of Elec. Eng.
Russell, Miss Ramona J., Computer Operator I
Seshu, Mrs. Lily H., 1/2 time Res. Asst.
Stephens, Allen F., Jr. Laboratory Mechanic
Taub, A. H., Res. Prof. of Appl. Math.
Wenta, Joseph M., Sr. Electronics Technician
Yu, Hwa-Nien, 1/2 time Res. Asst.

Student Assistants

Chan, Saifook (resigned May 28)
Dean, Floyd R.
Geis, John P.
Goodman, Robert
Kirwan, John F.
Ogata, Albert I.
Naumczik, George (started May 3)

The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, D. G. Gillies, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

R. E. Meagher.

R. E. Meagher

REM/hc

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

June, 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415. This contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contract N6ori-07130 and Contract N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

During the past year the Laboratory has been working on research on circuits and logical design for a very high-speed computing machine. Effective June 1, a contract sponsored jointly by the Atomic Energy Commission and the Office of Naval Research will make it possible to devote more of the Laboratory's effort to this program. The program generally intends to study both theoretically and experimentally a high-speed computer using direct-coupled asynchronous circuits with binary operation times from one state to another of about 25 mμs. In order to summarize the scope of the work which the Laboratory has in mind, the following three sections have been extracted from the proposal to the Atomic Energy Commission covering this work.

Circuits

During the summer and fall of 1955 the Laboratory has investigated circuits using both vacuum tubes and transistors with operation times of less than 50 millimicroseconds. An operation time here is taken to mean the total time to change from one binary state to another, starting from the beginning of a signal and ending with sufficient output signal to actuate the next operation. An operation time is the time which is additive for elementary circuits when a serial sequence of operations is considered. It includes all delays due to any cause. An operation time is to be distinguished from a rise time which would ordinarily be shorter. Several circuits are probably satisfactory in this speed range using either vacuum tubes or transistors. Recently the α-cutoff frequency of junction transistors has increased to a high enough value to make them appear more promising. Figure 1 shows a flipflop and gate circuit which has been tested with an operation time of about 21 mμs using surface-barrier transistors. This circuit has not been completely analyzed for tolerances and neither has a

complete set of appropriate, and, or and not circuits. Calculations on individual circuits and experiments on them indicate that circuits of this speed can probably be achieved. As a part of this proposal a set of circuits with operation times of 25 mμs or less would be worked on with the intention of using them in a general purpose machine. This circuit work has been carried out with the support of the Office of Naval Research.

The operation time for circuits of the type used in Institute for Advanced Study type machines such as the Illiac, is about 1.0 microsecond. Thus the elementary circuits proposed here are 40 times faster than the elementary circuits used in the Illiac.

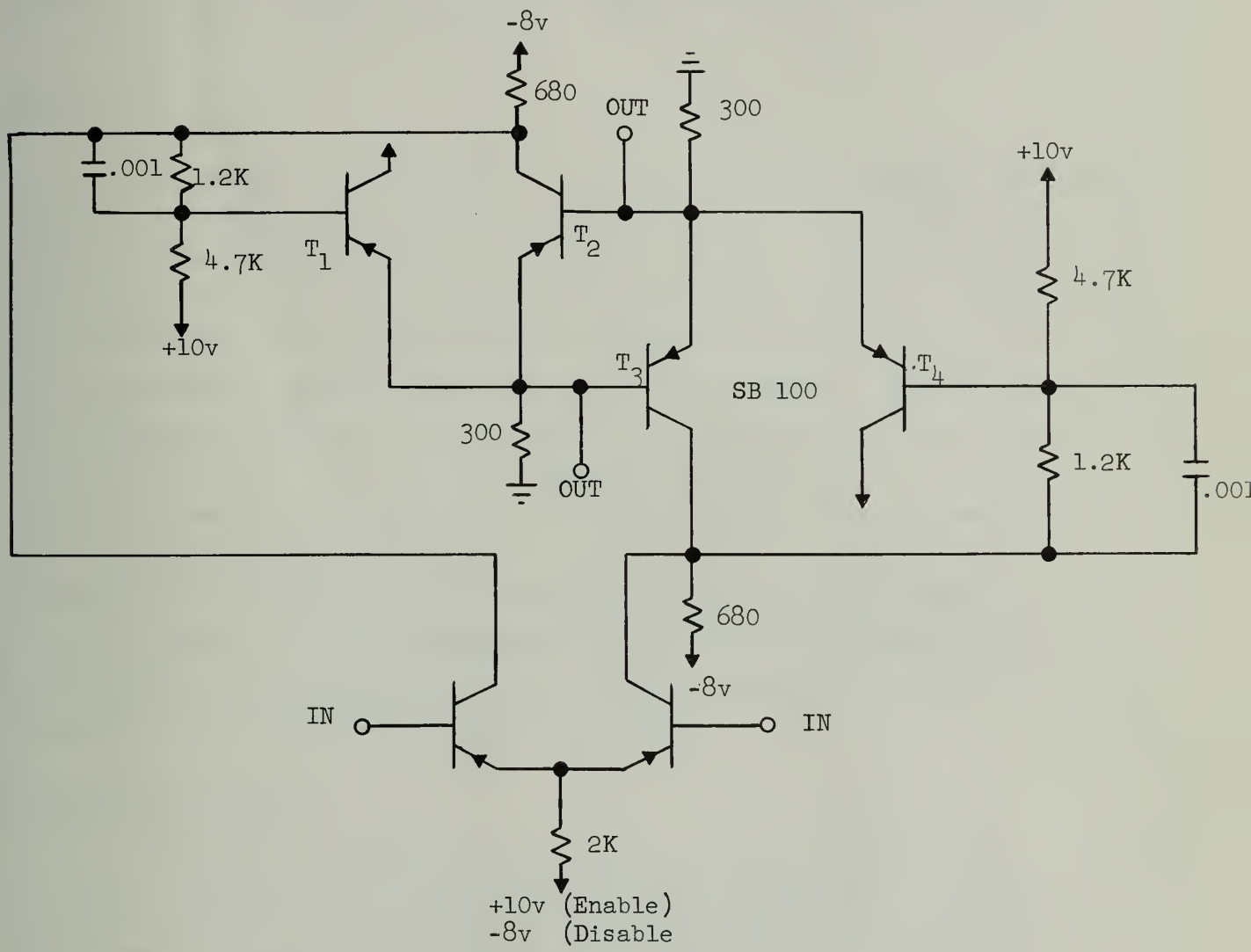

Figure 1

Crosscoupled Flipflop using Surface Barrier Transistors
Operation Time: About 20 millimicroseconds to 50% point.

A linear dimension of a final machine could be imagined to be as much as 3 meters. Since the velocity of light is 3×10^{10} cm./sec. the resulting transit time under the most favorable circumstances would be 10^{-8} second. Thus the proposed circuits would have operation times only 2-1/2 times as long as 10^{-8} second and it is clear that some attention will need to be applied to keeping the machine small. Since the circuits are expected to be asynchronous, at least in part, the dimensions of the machine, if large, will tend to slow up those operations which require the information to go over the whole dimension of the machine. Register operations may be included in this group but the effect on speed should not be large. Of course, every effort will be made to keep the physical machine as small as possible.

Form of Circuits

The logical interconnections of a computer can be classified as being ac coupled or dc coupled and synchronous or asynchronous. Most machines have been largely ac coupled and synchronous in nature. The most important exception to this is the I.A.S. group of machines which are at least partly dc coupled and in part asynchronous. The Digital Computer Laboratory at the University of Illinois has concentrated on asynchronous work in all of its efforts. Work on the algebra for this type of logic has been carried out. The experience of the Laboratory in using this type of logic has indicated that it contributes to reliability although reliability is a hard thing to measure and other factors besides the direct-coupled asynchronous features contribute to it. Asynchronous circuits, although harder to design, may be readily serviced. The asynchronous type of circuit and logic obviate the problems arising due to the information transit time discussed in the previous section. The asynchronous logical work has been supported in part by the Office of Naval Research.

Machine Organization

The design of a machine with a particularly fast arithmetic unit and with presently available memory systems poses serious organizational problems to prevent making the arithmetic unit wait for the memory. This will make necessary a study of the organization of the machine to make the most use of the speed of the arithmetic unit. The use of one or more additional registers would make it

possible to do more operations without referral to the high-speed memory. An important new instruction would be one that can combine an addition and a multiplication in one operation.

Balance of Memory and Arithmetic Unit

A study was made of the cost in time that would be paid in solving a problem of the type described below if a very high-speed computer was assumed to have a modest sized low access time memory and a large high-access time back-up memory in contrast to a large capacity low-access time memory. The type of problem considered was assumed to have the following characteristics: N words could be used to calculate N - k words which replaced an equal number of the original words and were used as the original words. The study was based on some remarks made by H. H. Goldstine in a private communication.

By assuming characteristics for the different access times that seemed in accordance with current engineering practices it was shown that the percentage increase in the time referred to above behaved essentially as

$$R = c\left(\beta_1 + \frac{\alpha_1/k + \beta_1/2}{N/k-1}\right)$$

It was then shown that in certain cases only a fifteen percent loss in computing time was the price paid from by an eight-fold decrease in the size of memory.

Transistor Test Computer

In June the transistor test computer was finally completed and it was possible to test some of its performance characteristics. As explained previously (see May, 1955, December, 1955, January-May, 1956 reports) this machine provides the proving ground for a set of dc-coupled transistorized logical elements having rise times of about 1 μs. The input-output impedance ratio of these units is sufficiently high (~ 10:1) to permit their use in all points without having to specify the load conditions. A complete report on this test unit is being prepared but a summary of some of its characteristics follows.

Machine Type:	Parallel, asynchronous, dc-coupled
Registers:	$A\bar{A}$ $Q\bar{Q}$ R^3R_3

Register Capacity:	4 binary digits
Memory:	Non-destructive core memory. 4 words, each one having 2 bits for the instruction and 4 for the number to be operated on.
Instruction Types:	Add, subtract, multiply, divide
Addition Time:	140 μs (including memory access)
Subtraction Time:	140 μs (including memory access)
Multiplication Time:	620 μs (including access and A→Q shift)
Division Time:	620 μs (including access and Q→A shift)
Number of Transistors:	752
Number of Diodes:	498
Power Consumption:	75W
"One"-level:	+2V (nominal)
"Zero"-level:	-2V (nominal)
Gating Voltage:	±4V (nominal)
Tolerances:	5% on supply voltages and resistors. $\alpha > .92$, $f_\alpha \geqslant 1$ MC.
Characteristic Rise-Times:	1 μs
Types of Plug-in Units:	Single-ended flipflop (F) and last moving point single-ended (F')
	Bridge modulator gate (G), combination with driver (G') power gate driver (P)
	Not-circuit (N), and level restorer (L)
	2 and 3 input and (A and A'), and or (O and O')
	Memory pulser (M), read-out amplifier (R), delay-circuit (Δ)
	Isolation diodes (D) and clear driver (C)

Experimental Tests on Speed-Independent Logic

Experimental work has been carried out on the design of several circuits including "A" chassis of the kind used in Illiac and binary counters which are believed to be strictly speed-independent as recently devised here. A program for Illiac has been used to analyze the speed-independence of circuits and several practical designs have been considered.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Continued Fraction Expansions

Study was made of a continued fraction routine for computing a large number of different functions. It uses a straightforward technique and makes use of the previously mentioned rational fraction routine for calculating exact coefficients. It is hoped that the study will lead to additional library programs which will have advantages in speed and memory requirements over the usual power series approximations to functions.

Magnetic Drum Use

Further work was done on the automatic use of the drum bootstrap with existing programs and in making some modifications of the input routines on the drum. The space requirement was shortened by about six words at the expense of introducing some additional complication into the calculation of key words. Since this calculation is done only once and is already complicated, the added complexity makes little difference.

Logical Design

The effects of a number of parameters of logical design (e.g., register arrangement, operation speeds, access time, complexity of instructions) are being studied by writing programs in various instruction codes.

Program Library

The following five programs were added to the library in June. Program V-7 was prepared by Professor W. C. Jacob of the Department of Agronomy.

V-7 (206) Provide Sets of Random Numbers From 1 to N. This is a program of the auxiliary library which uses V-3 to provide pseudo-random numbers and selects sets from them.

P-16 (214) Infraprint. 56 Words. This is an integer or fraction print routine which will print exactly rounded fractions or exact integers to n decimal places where $1 \leq n \leq 12$. It may be entered in any of 8 ways with a standard entry to provide a variety of kinds of output.

N-11 (215) Input a Sequence of Fractions or Integers. 25 Words. This program will read n place signed decimal numbers with $0 \leq n \leq 12$ from the tape. Fractions are correctly rounded on conversion with an error not exceeding 2^{-40} and integers are converted exactly.

Q-3 (217) Complete Circuit Analyzer. Complete Program. This is a program of the auxiliary library. It is designed to aid in the study of speed-independent circuits and analyzes complete circuits for speed-independence when given a description of the nodal equations and the initial state. The routine is limited to circuits with 39 nodes and having no more than $(703 - 4n - k)/6$ states per cycle; n is the number of nodes and k is the number of integers and plus signs required to describe the circuit. Only in extreme cases is more than 10 minutes required by the program.

X-1 (218) Decimal Order Input. 25 Words. This is a modification of the Illiac standard input routine. It is stored on the magnetic drum and need not be included on any program tape. It is faster than the old version (serial number 18) and provides room for one more parameter by reducing the number of temporary storage locations to two. Entries to it are as before except for one little-used one and it occupies the same memory positions as the old version.

PART III

ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-1221.)

Work is progressing on a code to integrate the Einstein field equations for a static, spherically-symmetric space-time in which there exists a perfect fluid whose caloric equation of state is arbitrary. The determination of these equations of state by the use of various distribution functions, which give the number of particles in a given volume of phase space, is under study. The purpose of this study is to rewrite the caloric equation of state so that the density is a function of pressure and another variable entering into the Einstein field equations.

A study has been initiated on the integration of the Einstein field equations for the gravitational fields due to a plane-symmetric distribution of a perfect fluid in adiabatic but non-isentropic motion.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During June specifications were presented for 19 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 908. Numbers followed by T are for theses.

809 T Chemistry. Electrostatic Deposition on Cylinders. Use of the Runge-Kutta method will be made to calculate trajectories for certain ranges of the variables and then an inverse interpolation will be used to select another boundary value. Results are given as collection efficiency.

810 T Education. Ethnocentrism and Rigidity Analysis. Standard programs in the Illiac and Psychology Program Libraries will be used to determine the relationships among ethnocentrism, rigidity, anxiety and social acceptability. Data have been collected on 160 students.

811 Electrical Engineering. Aperture Distribution. A number of integrals will be evaluated to calculate the field due to a uniform plane wave in a long narrow slot in an infinite conducting plane.

812 T Psychology. A Psychophysical Investigation of Triangular Form. Standard library routines will be used to estimate the projections of each of a set of triangles on k "psychological dimensions" in a euclidean space. The values on each dimension will be predicted from a set of physical measures of the triangles using a linear regression equation.

813 Bureau of Economic and Business Research. Illinois Employers Labor Force Anticipation. Library Routine K-12 will be used to obtain the necessary correlation coefficients to explain the factors influencing the labor force anticipations of Illinois employers.

814 T Electrical Engineering. Calculation of Surface Brightness. An equivalent electrical network is used to represent the light flux and its corresponding interreflections within an enclosure. Surface brightnesses are obtained by solving this network, the solution being obtained from sets of simultaneous linear equations.

815 Psychology. D-Statistic. This is a profile analysis with 20 items per profile and 8 profiles per subject.

816 Physics. AG-Cyclotron. This is a study of radial oscillation in a spiral ridge cyclotron. Runge-Kutta integrations will be carried along orbits with several different sets of boundary conditions.

817 Electrical Engineering. Depth of Penetration. The problem is an antenna study in which the depth of penetration is calculated as a function of 3 parameters.

818 Illinois Department of Public Welfare. Child Personality Structure. Data for this problem were gathered from a large number of 6-8 year old school children. They will be analyzed with centroid factor analyses and rotation procedures with the results being plotted with the cathode ray tube output.

819 Computer. Verify Transistor Flipflop. The program evaluates the maximum range of output levels for given tolerances, supply voltages, and resistor values. The computation consists of the evaluation of a set of 5 algebraic formulas.

820 State Water Survey. Precipitable Water Inflow for the State of Illinois. Data from 4 weather stations are used to compute and check precipitable water inflow, with 3 stations yielding data to compute inflow, and the last being used to check obtained data.

821 Chemistry. Charge Distribution in Molecules. The problem consists of calculating multipoles of the charge distribution of molecules using molecular orbital wave functions which are linear combinations of Slater atomic orbitals. The calculation is done in two stages; the first involving moment integrals and the second involving solution of matrix equations.

822 T Electrical Engineering. Location of the Roots of the Minimum Function. The problem is concerned with the locations of poles and zeros of the minumum function.

823 T Institute of Communications Research. A Comparison of Semantic Judgements for Two Cultural Groups. Osgood's Semantic Differential will be used to investigate the semantic judgements of Japanese and American cultural groups. The problem is essentially a series of factor analyses, between the two groups and between sexes within each group.

824 T Agricultural Economics. Farm Planning in Southern Illinois. Linear Programming Routine M-15 will be used to develop farm plans for typical farms in southern Illinois. Emphasis will be placed on various dairy alternatives.

825 Physics. Meson Phase Shift Determination. A set of five simultaneous non-linear equations are to be solved by determining the minimum of a function of the five-phase shifts. The minimization will be carried out with Library Routine H-5.

826 Electrical Engineering. Polynomial Coefficients. This program is used to calculate the coefficients of the polynomial obtained from the continued fraction expansion of a ladder network.

827 T Agricultural Economics. Soil Bank Study. Library Routine M-15 will be used to determine benefits from compliance with government soil-bank programs on typical farms in northern Illinois.

Table I shows distribution of machine time for the month of June.

TABLE I

Regular Maintenance and Engineering	42:14
Unscheduled Maintenance	17:15
Drum Engineering	32:03
R.A.R.	6:58
Leapfrog	43:20
Wasted	:16

TABLE I (Cont.)

Use by Departments

Computer Group	10:27
Physics	38:31
Control Systems Lab.	67:13
Structural Research	4:23
Struct. Res. (AF 24994)	5:45
T.A.M. (Task 53)	2:31
Psychology	22:23
Psychology (MD 569)	1:39
Electrical Engineering	12:58
Elec. Eng. (AF 3220)	2:31
Chemistry	34:46
Agriculture	18:42
MURA	159:55
Inst. Comm. Res.	6:19
Elec. Eng. (Nobs 64732)	2:07
Dairy Science (9B1-B2)	:05
Ill. Public Welfare Dept. (44-32-66-342)	2:21
Ill. Public Welfare Dept. (Hurley)	1:19
Demonstrations	1:20
Miscellaneous	18:59
	556:20

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M. and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M., and 7:00 A.M. the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind,

a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for June.

TABLE III

Drum	3
Control	2
Arithmetic Unit	3
Input-Output Unit	0
Punch	4
Reader	4
Memory	3
Power Supply	2
Unknown	6
Total	27

Comments on Auxiliary Drum Memory

During the month the head to drum spacing was decreased in such a way that the center-to-peak signal voltage from each head increased from 50 mv to

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/1/56	19:59	:01	1	(1) Two different results from same tapes	:00	:43	0
6/4/56	20:00	:00	0		:00	:51	0
6/5/56	19:57	:03	3	(1) Drum won't stay in synch. (2) " " " " " (3) Drum failure	:00	:58	0
6/6/56	19:57	:01	1	(1) 42 changed to 4K on R.H. side	:02	1:07	0
6/7/56	20:00	:00	0		:00	:43	0
6/8/56	20:00	:00	0		:00	:50	0
6/11/56	20:00	:00	0		:00	:50	0
6/12/56	20:00	:00	0		:00	1:27	0
6/13/56	20:00	:00	0		:00	1:11	0
6/14/56	20:00	:00	0		:00	1:08	0
6/15/56	20:00	:00	0		:00	1:20	0
6/18/56	19:45	:09	1	(1) Hangs up on 0-leftshift when reading in. Suspect white switch.	:00	1:07	0
6/19/56	17:31	2:25	4	(1) Two different results from same tapes. (2) Unknown error but a.c. line voltage is believed to have changed. (3) Memory error 0-1 position 2^{-24} (4) -300V. Drum power supply failure	:04	:38	0
6/20/56	17:01	2:59	4	(1) Two different results from same tapes. (2) Punch "5" punched a K as an F (3) Suspect Reader K error (4) Leapfrog failed, Memory position 2^{-24}	:00	1:02	1
6/21/56	16:41	3:19	3	(1) Hang-up when started due to white switch (2) Hanging up (Leapfrog) broken wire to "B" gate on punch (3) Leapfrog failure indicated a punch "5" error.	:00	:45	1

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/22/56	18:49	1:11	4	(1) Tube failure (5844) in RI (2) Leapfrog due to reader "J" (3) -300V. Illiac power supply failure. (4) Leapfrog failure due to tube failure in RI	:00	2:13	2
6/25/56	19:32	:27	2	(1) Punch "3" not punching clean holes (2) Reader "B" bulb burned out.	:00	1:04	1
6/26/56	15:13	4:47	3	(1) Leapfrog failed, wouldn't print out. Sum check incorrect. (2) Two different results from same tape. (3) Tube failure in RI same as noted 6-22	:00	:58	2
6/27/56	19:59	:01	1	(1) Two different results from same tapes	:00	:51	0
6/28/56	20:00	:00	0		:00	1:01	0
6/29/56	20:00	:00	0		:00	1:26	0
TOTALS	404:24	15:23	27		13	22:13	6

60 mv for a 40 KC signal. As a result, intermittent drum test code failures caused by crosstalk were eliminated and the average gain tolerance ratio increased from 2.0 to 3.3.

A thermoswitch was installed on the drum shell and the drum ac turn-on circuits were modified so that the drum motor is stopped if either the shell temperature rises to 38° or if the cooling unit blower is turned off.

Personnel

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate
Bartky, W. Scott, 1/2 time Res. Asst.
Black, Billie G., Draftsman
Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
Clements, Virgil F., Jr. Laboratory Mechanic
Conger, Richard A., Computer Operator I (started June 18)
DeWit, Roland, 1/2 time Res. Asst. (Resigned June 15)
Ehmen, Mrs. M. Gwendolyn, Computer Teletype Operator (Resigned June 29)
Farrington, Carl C., 1/2 time Res. Asst. (Resigned June 30)
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Wells, Mary Lou, Computer Teletype Operator (Started June 15)
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Student Assistants

Dean, Floyd R. (Resigned June 22)
Goodman, Robert
Motts, Clyde (Started June 21)
Naumczik, George

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McKay, R. W., Assoc. Prof. of Physics (for one year beginning July 1)
Gotlieb, C. C., Assoc. Prof. of Physics (for one month beginning July 1)

The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, D. B. Gillies, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

Part I: Study Program on High Speed Computer

Part II: Mathematical Research and Programming

Part III: Illiac Use and Operation - General Laboratory Information

(Most vacations in the Digital Computer Laboratory are being taken during the months of July and August.)

July, 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

Speed-Independent Circuits

In the last few months, work has been carried out in the Laboratory on the theory of speed-independence or asynchronous logic. This work has resulted in Laboratory Reports No. 66, "Theory of Asynchronous Circuits" by David E. Muller, and No. 71, "Speed-Independent Counting Circuits" by James C. Nelson, and Illiac Library Routine Q-3, "Complete Circuit Analyzer" by W. S. Bartky.

These reports indicated that some truly speed-independent circuits which were fairly simple were possible, provided that one or more special circuit elements could be devised. One of these circuit elements was called the C-element in Report No. 66. A physical electronic circuit with the properties of the complement of the C-element ($\overline{C}$-element) has been devised. This circuit is shown in Figure 1 and uses a single input-single output kind of flipflop which has been used here before on the transistor test computer with an adapter circuit. The element is shown in Figure 1. The $\overline{C}$-element is one such that if both inputs are "1" the output is "0"; if both inputs are "0" the output is "1". If the inputs differ, then the output agrees with the output of the previous state of the element.

The $\overline{C}$-element has been experimentally used in a three-phase speed-independent logical oscillator. The logical diagram for this circuit was first shown in Report No. 71 and has now been built and made to work. The circuit provides a logical oscillator which is truly speed-independent. It is possible to slow up the output of any point of the circuit for example by a capacitor, without interfering with the operation of the oscillator.

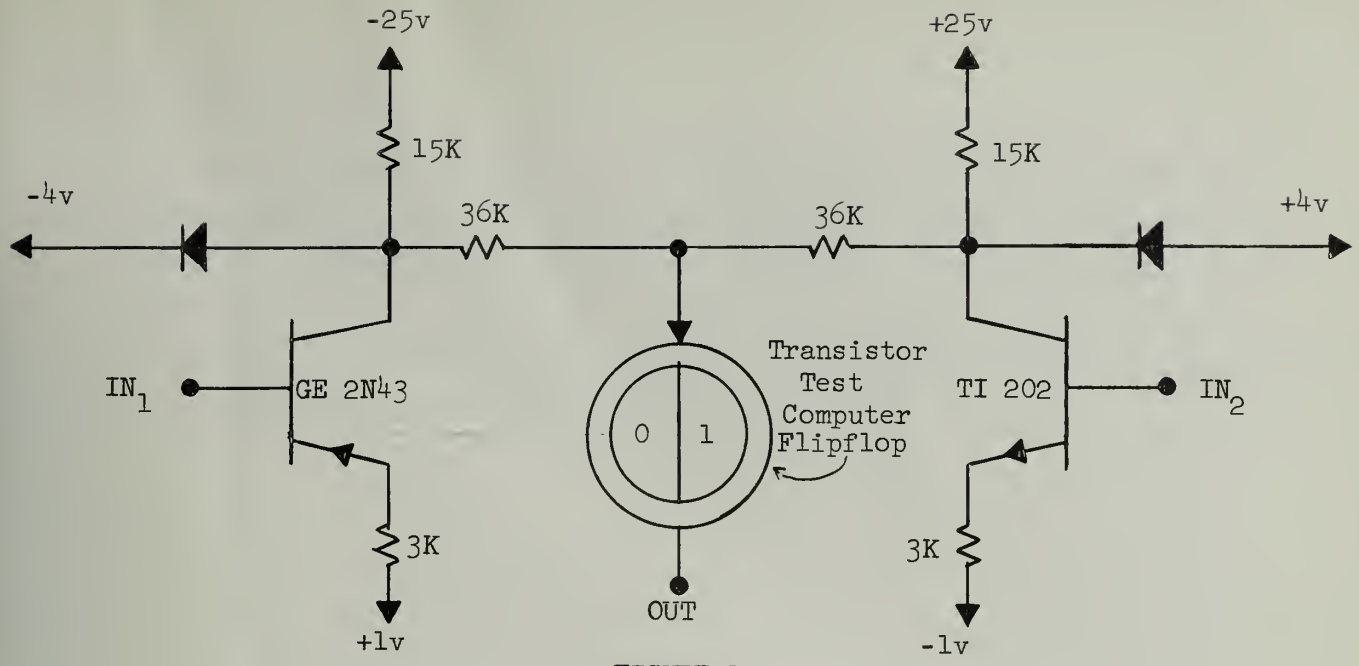

FIGURE 1

Circuit of a $\overline{C}$-Element

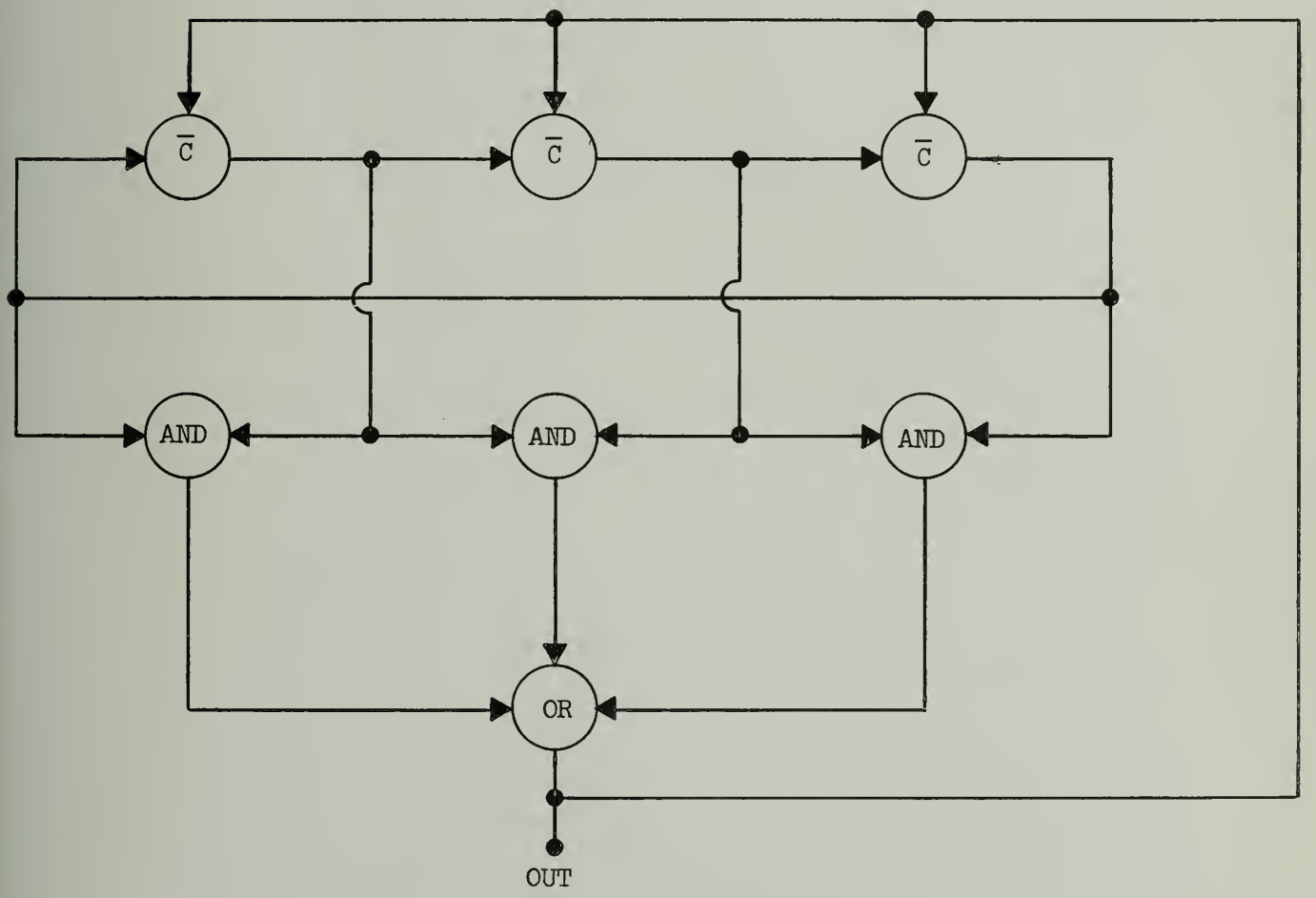

Figure 2

Logical Layout of a Three-Phase
Speed-Independent Logical Oscillator

Transistor Test Computer

The transistor test computer was put into operation during the month. There was one error-free run of 55 hours which was terminated by a flipflop failure when one transistor had an α-drop to about .85. Some additional changes will be made, which, it is hoped, will provide very long error-free runs. As reported earlier, the transistor test computer is a computer which uses asynchronous circuits constructed of one megacycle transistors.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Logical Design

We may conceive of a modification of the Illiac by adding additional S-registers in the arithmetic unit. An S-register may be connected when desirable to the adder in place of R^3 and may be connected to the accumulator in place of the memory.

A partial order code for a proposed automatic computer (PAC) which employs the use of additional S registers was designed and applied to several Illiac programs. The logic and current features of Illiac were maintained as far as possible in PAC, the major changes initiated being:

(1) addition of S registers

(2) circulation of the Q register

(3) addition of 3 B-boxes.

Three models of PAC are being considered: PAC-1, PAC-2 and PAC-3, the digits indicating the number of S registers assigned. A program was taken from the Illiac library, programmed for PAC-1-2-3 and these four programs were then compared on the basis of words, order accesses, instruction accesses and temporary storage. This was repeated for several programs, and it is planned to do this for a total of 8 or 10 programs. The qualities looked for in the programs selected are length, which must be reasonably moderate, frequency of use, and the loops and operations employed, which should be those most commonly used in programming. In some cases parts of programs, rather than entire programs were used. Although this does not offer a fair basis for comparison of computers, it is valuable in that those parts, which might otherwise be ignored because they are imbedded in lengthy programs, suggest new instructions which might be desirable in PAC.

Some results of this work follow. The columns are headed: words (W), order accesses (OA), instruction accesses (IA) and temporary storage (TS). Here an order access is defined as the time required to transfer a word from the store to the arithmetic unit or vice-versa while an instruction access is defined as the time required to transfer a word from the store to the order register.

1. Square Root: R-1 (Newton's Method)

	W	OA	IA	TS
Illiac	9	4 + 6n	4 + 5n	3
PAC-1	9	3 + 2n	4 + 5n	2
PAC-2	8	1 + n	3 + 5n	1
PAC-3	8	1	3 + 5n	0

(1) n = number of iterations.

2. Scalar Multiplication with Overflow Check (from M-6)

	W	OA	IA	TS
Illiac	11-1/2	10k	9k	2
PAC-1	9	2k	(5 to 7)k	0
PAC-2, PAC-3	not needed			

(1) k is defined by $c_{ij} = \sum_k a_{ik} b_{kj}$

(2) This is the 11-1/2 word loop which actually performs the scalar multiplication in M-6.

3. Exponential: S-2 (Polynomial Evaluation)

	W	OA	IA	TS
Illiac	17 programs 16 constants	19 + (5)·8	15 + (5)·5	2
PAC-1	12 programs 15 constants	10 + (5)·1	10 + (5)·2	1
PAC-2	12 programs 14 constants	8 + (4)·1	10 + (4)·2	1
PAC-3	12 programs 14 constants	6 + (4)·1	10 + (4)·2	0

(1) The number in parentheses under OA and IA is the number of passes through the polynomial loop used to evaluate an exponential.

(2) The Illiac program uses the old method of setting the link(i.e. does not use K-5) which necessitates a waste order. Therefore the number of program words should really be 16 instead of 17.

The problem of code-checking becomes much greater when B-registers are used because less information is stored. A study is being made of this problem to help decide what instructions might be useful in checking and what hardware might be desirable to make code-checking easier.

Program Library

The following routine, prepared by Judith Blankfield for the Department of Electrical Engineering, was added to the Auxiliary Library.

V-18 (219) Ordinary Bessel Functions. 257 Words. This is a routine for calculating Bessel functions J_n and Y_n of the first and second kinds. An input parameter is used to specify which kind or kinds shall be calculated and whether the order is to be first or second or a combination. For example, one may compute J_o alone or J_o and J_1 or J_o and Y_o, etc. The accuracy is about 4 decimal places and the time at most 100 milliseconds.

PART III

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During July a new procedure was introduced for the running of small standard problems. Problem specifications and code checks are no longer required for running any of the problems listed below provided that

(a) the time required is 15 minutes or less,

(b) parameters and data are furnished on a single tape,

(c) use is made of the operator's copy of the program.

A minimum of formality is thus required to solve short problems using the following programs:

J-2	Roots of a Polynomial
K-2	Product Moment Correlations
K-8	Product Moments (Drum)
K-9	Product Moments (Log Scale)
K-12	Multiple Regression
K-13	Analysis of Variance
L-2	Simultaneous Equations
M-12	Matrix Triangularization
M-13	Equation Solver and Inversion
M-18	Eigenvalues and Eigenvectors

During July specifications were presented for 28 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 828. Numbers followed by T are for theses.

828 MURA. Partial Differential Equation. The Illiac will be used for solution of the Dirichlet problem for a second-order elliptic partial differential equation in two variables by an iterative method. The problem will be solved for many different domains and boundary values.

829 Psychology. Factor Structure of Anxiety Responses. Three 90 by 90 correlation matrices will be calculated and analyzed by the centroid method of factor analysis. A simple structure will be sought by use of the oblimax method and plotting with the cathode ray tube output.

830 Illinois State Geological Survey. Mixed-Layer Effects in Rhombohedral Carbonates. The problem is concerned with the computation of predicted X-ray diffraction diagrams for crystals made up of two kinds of atomic layers present in varying proportions and with varying probabilities of alternating with each other. Intensity from a single layer is computed from an exponential expression and the result from a succession of layers is obtained from a Markov chain model.

831 College of Medicine. Attitudes Toward Neurotic Children. Standard factor analysis routines from the Illiac and Psychology Program Libraries will be used to study the types of children that develop psychosomatic illnesses.

832 Computer. Frequency Analysis of Instructions and References to Store. This will be a study of the relative frequency of occurrence of different instructions and the frequency of references to storage locations for programs in the Illiac Library.

833 Electrical Engineering. Pattern of an Antenna in Front of a Conducting Screen. The relation for the pattern will be evaluated for a wide range of values of the three parameters giving azimuth, elevation and wavelength.

834 T University of Michigan Psychology Department. Factorization of Psychological Variables. The Psychology program for estimation of communalities will be used to factor analyze a 75-variable correlation matrix. The purpose of the study is to identify the underlying dimensions of a number of tests among which are personality tests, social perception tests, vocational interest tests, economic interest tests, political interest tests, and humor preference tests.

835 Computer. Quotient of Two Polynomials. This program will evaluate the quotient $P(j\omega)/Q(j\omega)$ where P and Q are complex polynomials of degree 63 or less.

836 Civil Engineering. Simultaneous Equations. This is a check program, using the Illiac routine, for solving a set of 140 simultaneous linear algebraic equations.

837 T Economics. Molasses Demand Study. This is a statistical analysis of the demand for industrial molasses using the single equation least squares approach and the limited information system of equations approach.

838 Washington State College. Fruit Demand Study. Library Routine K-12 will be used to make a study of the demand of consumers for fruit as the season progresses. Data were taken on prices and quantities as well as quality and appearance for a number of fruits.

839 T Civil Engineering. Non-uniform Torsion of Bow Girders. Finite difference methods will be used to reduce the governing differential equations to sets of simultaneous linear algebraic equations which will be solved by one of the Illiac library programs.

840 Psychology. Analyses of Biological Correlations. This study is concerned with the applications of factor analysis to biology. A comparative study will be made with a series of correlation matrices ranging from size 10 by 10 to size 18 by 18 and dealing with characteristics of flies, aphids and bees.

841 University High School. Analysis of Mathematics Project Data. Standard library routines will be used to calculate product moments and to carry out some computations involving a covariance matrix. Data are scores on tests of various mathematical abilities collected from 500 high school students participating in the University of Illinois School Mathematics project.

842 T Physical Education. Relationship Between Body Structure and Weight Lifting Activities. The object of this study is to obtain prediction equations which will make it possible to predict performance from body measures. Twenty-seven body measurements and ten performance measures have been obtained on 241 subjects.

843 Electrical Engineering. Ladder Network Analysis. The problem is, given a ladder network, to calculate the impedance. The analysis is to be carried out in floating arithmetic and will consist of calculating the coefficients of two polynomials and then finding the roots of the polynomials.

844 T Physical Education. Study of the Primary Components of Cardiovascular Tests. The study is directed at determining the relationship between cardiovascular tests in young boys seven to fifteen years of age and of determining the primary factors involved in the relationship. The analysis will make use of library routines.

845 Chemistry. Data Fitting. An empirical equation is to be determined from data consisting of molar extinction coefficients of a solution in which several first-order chemical reactions are taking place.

846 T Electrical Engineering. Network Analysis. The problem is concerned with the determination of the poles and zeros of an equation which is given as a function of five parameters.

847 T Dairy Science. Effects of Weather on Daily Milk Production. Observations on daily milk and fat production were collected in a dairy herd at ten-day intervals during the summer months for the past five years. Also recorded were the maximum and minimum temperatures, relative humidity, and wind velocity for each of the sample days and for the three days preceding the sample day. The effect of each of the factors and of combinations of them will be studied.

848 University of Michigan Psychology Department. Study of Marital History Variables. This is a factor analysis problem in which data were obtained from a study of 300 engaged couples assessed on about 400 variables. The study began 20 years ago and the subsequent marital history has been followed, most of the original subjects being re-tested after 20 years of marriage.

849 T Psychology. Dimensionalization of Difficulty. Messick's technique is used to obtain scalar distances between pairs of words on data obtained when a list of 14 words was given to each of two groups of 40 subjects.

850 T Dairy Science. Seminal Characteristics of Dairy Cattle. Thirteen characteristics were observed twice weekly over a period of one year. Library Routine K-2 will be used to analyze the data.

851 T Agricultural Economics. Supply and Demand for Milk. Library Routine K-12 will be used to solve a 3-variable multiple correlation problem to show the influence of income and price upon the per capita milk consumption. A simple correlation of milk prices and milk production will also be carried out.

852 Economics. Optimal Partitition of Discrete Points. The original economic problem is to divide a population into groups or categories such that members within the same group are homogeneous in the sense of having numerical measures nearly the same. The problem differs from analysis of variance and other classification problems in statistics in that the groups are not defined in advance but are defined as a result of solving the problem. The method of solution is to have the Illiac systematically identify, list and compute values for certain relevant partitions, reducing the number by application of several basic principles.

853 Physics. Processing of Superconduction Transition Data. Experimental data consist of a sequence of 31 numbers which must be summed and normalized and then plotted. The Illiac will be used to carry out the computations with the results being plotted and photographed on the cathode ray tube output.

854 T Civil Engineering. Natural Frequency with Rotational Restraint. The problem is an extension of structural frequency analysis which generally has a determinantal equation of nth order corresponding to n degrees of freedom. Inclusion of rotational restraint at the base requires a system having n+1 degrees of freedom.

855 T Electrical Engineering. Calculation of Network Function. From the topological relations of a network it is possible to write an expression for the driving point function, to pick all possible combinations of v-1 elements (where v is the number of vertices in the network), and determine whether or not they represent a tree of the network.

Table I shows distribution of machine time for the month of July.

TABLE I

Regular Maintenance and Illiac Engineering	38:11
Unscheduled Maintenance	8:56
Drum Engineering	30:06
R.A.R.	6:15
Leapfrog	40:32
Wasted	:06
<u>Use by Departments</u>	
Computer Group	17:50
Physics	37:00
Control Systems Lab.	87:27
Structural Research	3:08
Struct. Res. (AF 24994)	13:46
T.A.M. (Task 53)	:25
Psychology	22:21
Psychology (MD 620)	4:32
Electrical Engineering	12:39
Elec. Eng. (AF 3220)	:05
Elec. Eng. (Nobs 1934(03))	1:40
Chemistry	28:07
Agriculture	23:16
MURA	114:14
Ill. Dept. of Pub. Welfare (Coan)	10:27
Ill. Dept. of Pub. Welfare (Hurley)	:39
Washington State College	6:17
University of Michigan	4:50
Demonstrations	1:06
Miscellaneous	31:17
	545:12

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 P.M. period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for July.

TABLE III

Reader Errors	7	White Switch Error	1
Punch Errors	7	Scope Output Errors	2
Drum Errors	3	Control Error	1
Power Supply	1	Power Line Failure	1
		Memory Error	1
	TOTAL INTERRUPTIONS AND ERRORS		24

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
7/2/56	19:59	:01	1	(1) Possibly reader "B" error	:00	:47	0
7/3/56	19:58	:02	2	(1) Reader "B", failed to read a "1" (2) Reader "B" error	:00	:43	0
7/5/56	20:00	:00	0		:00	:54	0
7/6/56	19:59	:01	1	(1) Drum error	:00	1:01	0
7/9/56	19:37	:23	1	(1) Bad photo cell in reader "B"	:02	1:13	0
7/10/56	19:56	:02	2	(1) White switch trouble (2) Drum failed	:02	1:41	0
7/11/56	19:26	:34	2	(1) Operator jammed punch (2) Leapfrog failed, punch "3" error	:00	1:47	1
7/12/56	19:58	:00	0		:02	:28	0
7/13/56	20:00	:00	0		:00	:50	0
7/16/56	19:57	:01	1	(1) Punch "5" error	:02	:41	0
7/17/56	19:13	:43	2	(1) Pos. C.R.T. output pulser fil. out (2) Control error. A 2C51 tube in even address gate chassis caused failure. This was not found, partly because of its intermittent nature, until July 24.	:04	:59	0
7/18/56	19:48	:10	0		:02	2:00	0
7/19/56	19:22	:38	2	(1) Punch "5" punched extra 4 holes (2) " "5" " " 4 "	:00	:56	1
7/20/56	20:00	:00	0		:00	:40	0
7/23/56	18:12	1:48	0		:00	1:04	0
7/24/56	19:37	:23	2	(1) Film jammed in cassette (2) 38 should have been 34 - C.R.T. Pos. 2^{-24}	:00	4:41	0
7/25/56	19:59	:01	1	(1) Drum failure	:00	:47	0
7/26/56	19:49	:11	2	(1) Drum power supply failed. Control rectifier filament burned out (2) Reader "B" coupling came loose	:00	:50	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
7/27/56	19:49	:11	3	(1) Power line failure (2) Reader "B" light out (3) Reader "K" error	:06	1:29	0
7/30/56	19:59	:01	1	(1) "A" gate on punch "5" burned out	:00	1:00	0
7/31/56	19:59	:01	1	(1) Operator error, jammed punch "5"	:00	:49	0
				Note: The control error listed on July 17 as error number 2 was not diagnosed and repaired until July 24. There were 9 more interruptions of work due to this one tube failure before the trouble was diagnosed. These nine interruptions are not listed as separate errors in this table.			
TOTALS	414:37	5:11	24		:12	22:20	2

Reports and Seminars

Laboratory Report No. 71, "Speed-Independent Counting Circuits," by James C. Nelson, July 1, 1956.

Personnel

The personnel associated with the group and hence the contributors to this report are:

Aronson, Donald G., Research Associate
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Student Assistants

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Motts, Clyde
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Gotlieb, C. C., Assoc. Prof. of Physics (for one month beginning July 1)

McKay, R. W., Assoc. Prof. of Physics (for one year beginning July 1)

The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, W. J. Poppelbaum, D. B. Gillies, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein

Part I: Study Program on High Speed Computer

Part II: Mathematical Research and Programming

Part III: Illiac Use and Operation - General Laboratory Information

(Most vacations in the Digital Computer Laboratory are being taken during the months of July and August.)

August, 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

Comments on Relative Memory Sizes

One estimate of the minimum time necessary for carrying out most computations is given by the product

$$m\ F\ M$$

where

m = number of multiplications in the problem

M = time for one multiplication

F = a factor varying between 2.5 and 7.5 for most problems.

For some problems the total number of multiplications satisfies the inequalities:

$$10^7 \leq m \leq 10^{11}$$

Such problems may require the use of 50,000 to 100,000 words of data. However, only small amounts of data are needed at any one stage of the computation. The question arises as to whether all these words need to be in the memory with access time a or whether some may be stored in "back-up" memories. We shall try to evaluate the time lost in using a back-up memory.

Suppose our problem is such that if N words of data are in the highest speed memory we may then calculate N-k new words which replace the same number of words previously held. Thus in one sweep through the memory N-k words are calculated and these may be stored in positions previously occupied by other words. If N-k is as large as required by the problem, this process is repeated many times and the total time for the calculation is

$$(N-k) \times n \times F \times M \times T = \tau_1 T$$

where

n = the number of multiplications for each of the $(N-k)$ words

T = the number of times the memory is swept through.

If however $N-k$ is not as large as required we must add to this the time necessary to load and unload the memory. Let us say that the time necessary to unload the high-speed memory is made up of two parts: (a) a time to get access to another memory, α and (b) a time to read $N-k$ words into this memory, $(N-k)\beta$.

Thus unloading time is

$$\alpha + (N-k)\beta.$$

Assuming that reading and writing in the latter memory take equal times and that we have to read N words from it in order to properly load the high-speed memory we have as our loading time

$$\alpha + N\beta.$$

Hence the total loading and unloading time is

$$2(\alpha + (N-k)\beta) + k\beta.$$

The ratio of this time to the computation time per load in the memory is

$$R = \frac{2(\alpha + (N-k)\beta) + k\beta}{(N-k)n\ F\ M}$$

$$R = \frac{2}{n\ F\ M}\left(\frac{\alpha + \frac{\beta k}{2}}{N - k} + \beta\right)$$

The total computation time is now

$$(1 + R)\ \tau_1 T\ .$$

Hence the ratio R is a measure of the cost of using a pair of memories instead of a single memory. We may write

$$\alpha/M = \alpha_1$$

$$\beta/M = \beta_1 \ .$$

Then

$$R = \frac{2}{n\,F}\left(\frac{\alpha_1 + \frac{\beta_1 k}{2}}{N - k} + \beta_1\right) = \frac{2}{n\,F}\left(\beta_1 + \frac{\alpha_1/k + \beta_1/2}{N/k - 1}\right)$$

In this formula n, N, and k depend on the problem being solved and α_1 and β_1 depend on the equipment being used. For a given problem we may estimate the size of high-speed memory N so that R is the order of 10%. The important thing to note is that the rate of change of R with N is a slowly varying function beyond the value of 10%.

Goldstine, in a private communication, has shown that a problem in hydrodynamics in which time and two spatial variables enter where 50,000 words of storage are needed an inner memory with room for 1750 words of data involves less than 10% of computing time for consulting the secondary memory, when

$$\alpha_1 = 1700 \text{ or less}$$

$$\beta_1 = .8 \text{ or less}$$

$$k = 500$$

$$n = 10$$

$$F = 5.$$

However Goldstine did not consider the complications ensuing when slip-streams occur in the computations.

Suppose now we examine the question as to whether a random access memory of 30,000 word capacity is needed.

In two and three dimensional hydrodynamics problems in which the quantities are time dependent, the amount of data which has to be processed in one time step will exceed this capacity by a factor which is at least between one and two and may be five. Therefore a back-up memory will be needed in any case. We are thus dealing with the factor R and the question is what is the value of R for $N \approx 30{,}000$ and say $N \approx 2{,}000$.

Suppose we have a drum in which

$$\alpha = 17000\ \mu\text{sec} = \text{access time to a word.}$$

$$\beta = 8\ \mu\text{sec} \quad = \text{read time for a word.}$$

If then our multiplication time is assumed to be 5 μsec

$$\alpha_1 = 3400$$

$$\beta_1 = 1.6$$

$$R = \frac{2}{nF}\left(1.6 + \frac{3400/k + .8}{N/k - 1}\right)$$

For k = 500

$$R = \frac{2}{nF}\left(1.6 + \frac{7.6}{N/500 - 1}\right)$$

$$R_{30000} = \frac{2}{nF}(1.7) = .068$$

$$R_{2000} = \frac{2}{nF}(3.6) = .144$$

when $2/nF = .04$, $(F = 5,\ n = 10)$.

Hence the ratio of the times to do the same problem with a memory of 32,768 words and one with 4768 words (2768 words of code being used) is

$$\frac{1.14}{1.07} = 1.07$$

A seven percent increase in time is gained by an almost eight-fold increase in size of memory.

For k = 1000 we have

$$R = \frac{2}{nF}\left(1.6 + \frac{4.2}{N/1000 - 1}\right)$$

$$R_{30000} = \frac{2}{nF}\left(1.6 + \frac{.42}{3}\right) = \frac{2}{nF}(1.74) = .07$$

$$R_{2000} = \frac{2}{nF}\left(1.6 + \frac{4.2}{1}\right) = \frac{2}{nF}(5.8) = .23$$

Here then we have a similar phenomenon. The ratio in times being

$$\frac{1.23}{1.07} = 1.15,$$

a fifteen percent loss in time being paid for by an almost eight-fold increase in size of memory. The doubling of the factor k, the amount of dead-weight data being carried in the transfers is responsible for the change in loss of time.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

The basic method of handling time in speed independent circuit theory has been changed so as to simplify all the initial development. This new treatment has removed all the difficulties mentioned in previous reports, and the complete theory is now in condition to be written up. A verbal description of the new theory was given in August at the Los Angeles meeting of the Association for Computing Machinery.

The theory in its abstract form deals with n dimensional vectors $a = (a(1), a(2), \ldots, a(n))$ whose components are zeros and ones (these vectors are called states) and with a set of n Boolean functions $z(i)' = f_i(z(1), z(2), \ldots, z(2))$ (which are called the circuit). We discuss "allowed" sequences of states $a_1, a_2, \ldots$ which satisfy two conditions:

1. For any consecutive pair of states a_j, a_{j+1} in an allowed sequence we have $a_j \neq a_{j+1}$ and $a_j' \oplus a_j \supset a_{j+1} \oplus a_j$.

2. There is no pair of integers i and j such that $a_k(i)' \neq a_k(i) = a_j(i)$ for all $k \geq j$.

Allowed sequences may be finite or infinite and are intended to represent the sequences of states through which an asynchronous circuit may pass when started in state a_1. The first important result is that at least one allowed sequence exists having any initial state a_1. Speed independence is now most conveniently defined with reference to allowed sequences as follows.

A circuit is speed independent with respect to an initial state a_1 if there exists a maximal set of states M (as defined in previous reports) such that at least one state in M is present in every allowed sequence starting with a_1.

This definition can be shown to be equivalent to the previous definition, and using the new theory we can show more easily that semi-modular circuits are speed independent. No previous results are invalidated by the new theory.

PART III

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

There are several combinations of function digits used for stop instructions on the Illiac, the combination FF being used for stops caused by programmed checks. Addresses have been assigned to all FF orders in programs, and a list is maintained so that the operator can readily determine the cause of a stop. For example, if the computer is stopped by FF 015, the data tape for Library Routine K-8 has the wrong number of variables. A stop by FF 013 signifies a drum transfer failure in Library Routine K-12. The list now has about 25 addresses.

During August specifications were presented for 12 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 856. Numbers followed by T are for theses.

856T Physics. Release of Stored Energy in Cold-Worked Metal Crystals. This problem uses the same program as that for problem number 750. In the present series of experiments the samples used are single crystals of pure copper, rather than polycrystals which were used previously.

857 Structural Research. Natural Frequencies of a Beam Simply Supported at Both Ends, with a Spring Support at a Distance. This is a variation of problem number 740 in which Library Routine H-1 for inverse interpolation is used to search for the natural frequency of a simply supported beam with a spring support at a distance from one end.

858 Physics. Probability of Counting Gamma Rays from the Decay of Pi^{o} Mesons. This problem is for the purpose of determining the efficiency with which a counter will detect mesons by counting its decay gamma rays. The principal part of the computation is concerned with the evaluation of a double integral, the results being printed in tabulated form.

859T Physics. Release of Stored Energy in Cold-Worked Cu Crystals. This is an entirely new program designed to do a more complete and efficient job of the work formerly done with problem 856T.

860 Chemistry. Random Walk of Polymers. The work on this problem is in connection with the determination of the equilibrium statistics of dilute polymer solutions. Monte Carlo methods are used to study the special distribution of such polymers.

861 Chemistry. Calculation of Vibrational Frequency of Three Centered Body. This problem is concerned with the development of a mathematical model to describe certain experimental results.

862 Michigan State University. Cam Dynamics. The problem to be solved here is, given the acceleration characteristics of a cam, to calculate a table of values specified on the cam contour. A table will also be calculated to specify the residual dynamic stresses in the follower system after one cam stroke. The basic computations consist of the evaluation of a definite integral by means of Simpson's rule.

863T Theoretical and Applied Mechanics. Buckling of Shell under Internal Pressure and Axial Compression. The problem is to determine the post-buckling, equilibrium configurations of a long cylindrical shell subjected to internal pressure and axial compression. The equilibrium configurations are obtained by minimizing the potential energy of the shell, the potential energy being described by a fourth degree polynomial in three displacement parameters and four other parameters involving thickness and wave length.

864 Structural Research. Stiffness of Carry-Over Factors for Orthotropic Plates. This investigation is concerned with the analysis of orthotropic plates simply supported along two opposite edges and continuous in other directions over a series of rigid or flexible supports transverse to the simply supported edges. The present program evaluates expressions for stiffness, carry-over factors and the product of these quantities, for values of the relative stiffness parameter less than one.

865T Chemical Engineering. Calculation of Average Interaction Energies. The evaluation of multiple integrals for the calculation of average interaction energies will be done either by Simpson's rule or by a Monte Carlo method.

866 Mechanical Engineering. Axially Symmetric Supersonic Flow. Various types of initial and boundary conditions will be studied in a solution of systems of self-iterating difference equations derived from a quasi-linear second order partial differential equation of hyperbolic type.

867 Structural Research. Analyses of Rectangular Orthotropic Plates. Ritz's approximate method is used to study the analysis of rectangular orthotropic plates fixed along the boundaries and subjected to a load uniform in one direction and linearly varying in the other. The program computes the coefficients in the systems of equations and uses a modified version of Library Routine L-2 for the solution.

Table I shows distribution of machine time for the month of August.

TABLE I

Regular Maintenance and Illiac Engineering	40:49
Unscheduled Maintenance	5:11
Drum Engineering	32:32
R.A.R.	5:41
Leapfrog	45:36
Wasted	:05

TABLE I (Cont.)

Use by Departments

Computer Group	15:11
Physics	33:38
Control Systems Laboratory	32:52
Structural Research	4:15
Struct. Res.(AF 24994)	5:46
Electrical Engineering	9:02
Elec. Eng. (Nobs 64723)	1:29
Elec. Eng. (Nobsr 1834(02))	:27
Psychology	10:04
Psychology (MD 620)	3:34
Chemistry	13:17
Agriculture	24:30
MURA	274:12
Ill. Dept. of Public Welfare (Coan)	4:54
Ill. Dept. of Public Welfare (Hurley)	1:33
Michigan State University	4:20
Demonstrations	:00
Miscellaneous	36:45
	605:43

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a

summary table has been prepared using the period between 11:00 and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for August.

TABLE III

Reader Errors	2
Punch Errors	2
Memory Errors	1
Drum Errors	6
Unknown	1
Film jammed in camera	1
TOTAL INTERRUPTIONS AND ERRORS	13

Personnel

The personnel associated with the group and hence the contributors to this report are:

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
8/1/56	19:59	:01	1	(1) 5th hole failed to punch on 5	00	1:15	0
8/2/56	19:59	:01	1	(1) Drum out of synch.	00	:41	0
8/3/56	20:00	:00	0		00	:43	0
8/6/56	19:31	:29	1	(1) Memory pos 2^{-24}	00	1:29	1
8/7/56	20:00	:00	0		00	1:06	0
8/8/56	19:57	:01	1	(1) Unknown error	02	1:14	0
8/9/56	19:44	:14	2	(1) Drum Failure (2) Drum Failure	02	:48	0
8/10/56	19:59	:01	1	(1) Reader "B" error	00	1:10	0
8/13/56	19:49	:11	2	(1) Drum Failed (2) Film jammed in camera	00	:55	0
8/14/56	20:00	:00	0		00	:52	0
8/15/56	20:00	:00	0		00	:42	0
8/16/56	19:59	:01	1	(1) Punch No. 5 jammed.	00	:39	0
8/17/56	20:00	:00	0		00	:48	0
8/20/56	20:00	:00	0		00	1:03	0
8/21/56	20:00	:00	0		00	1:15	0
8/22/56	19:25	:35	1	(1) Drum and white switch trouble	00	1:06	0
8/23/56	20:00	:00	0		00	:40	0
8/24/56	20:00	:00	0		00	:48	0
8/27/56	20:00	:00	0		00	:43	0
8/28/56	20:00	:00	0		00	:56	0
8/29/56	20:00	:00	0		00	:28	0
8/30/56	19:59	:01	1	(1) Drum error	00	1:30	0
8/31/56	19:59	:01	1	(1) Reader "B" error	00	1:16	0
TOTALS	458:20	1:36	13		04	22:07	1

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Bartky, W. Scott, Research Assistant (Term. 8-15)
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Conger, Richard, Computer Operator I
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Holm, Walter H., Jr. Electronics Technician
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Kemp, John C., 1/2 time Research Assistant
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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

September, 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415. This contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contract N6ori-07130 and Contract N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

High Speed Memory

Conventional magnetic-core memories have cycle times not shorter than about 6 microseconds. The main factor fixing this minimum time is the limitation placed on the currents used by the method of selecting a particular core to read or store information. Figure 1 without the dotted lines shows one digit-plane of a con-

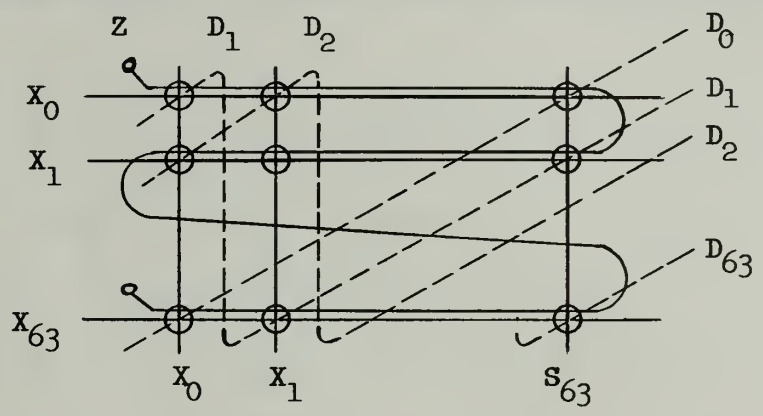

Figure 1. Digit-Plane Windings
(Sensing winding not shown)

ventional memory. Figure 2 shows the waveform of currents in one X and one Y winding and in the Z winding which passes through all cores of the digit-plane.

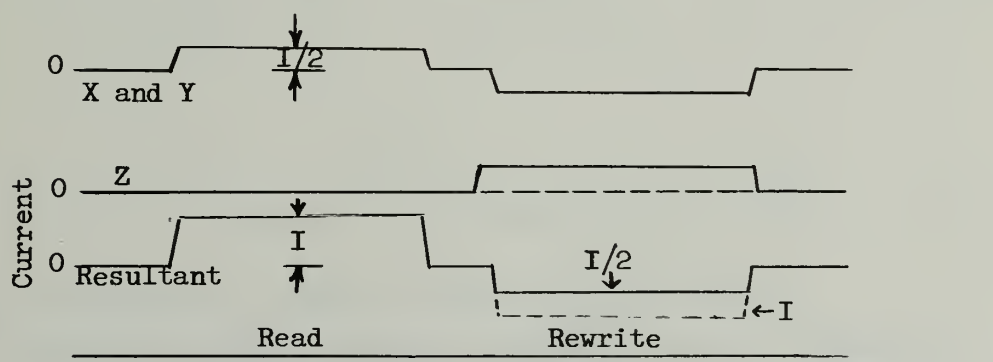

Figure 2. 2:1 Selection Ratio
(Full line rewrite 0
Dotted line rewrite 1)

The core at the intersection of the chosen X and Y winding has a resultant current I during the "read" pulse as shown in the bottom graph. Any other core on the chosen X winding or Y winding will have a current I/2 which must not be sufficient to alter permanently the magnetic state of the core. Thus the "selection ratio" (i.e. the ratio of current in the selected core to the maximum current in any other core) is 2:1. On the "rewrite" pulse the Z winding carries a current of 0 or +I/2 depending on whether a "1" or a "0" is to be stored. Again the selection ratio is 2:1.

Methods of arranging windings to give an n:1 selection ratio have been suggested[1] and some work has been done with a 3:1 ratio,[2] but no attempt has been described to apply these methods to the design of a memory faster than 6 microseconds.

One arrangement giving a 5:1 selection ratio is shown in Figure 1 with the dotted lines and Figure 3. The X, Y, and D windings are so arranged

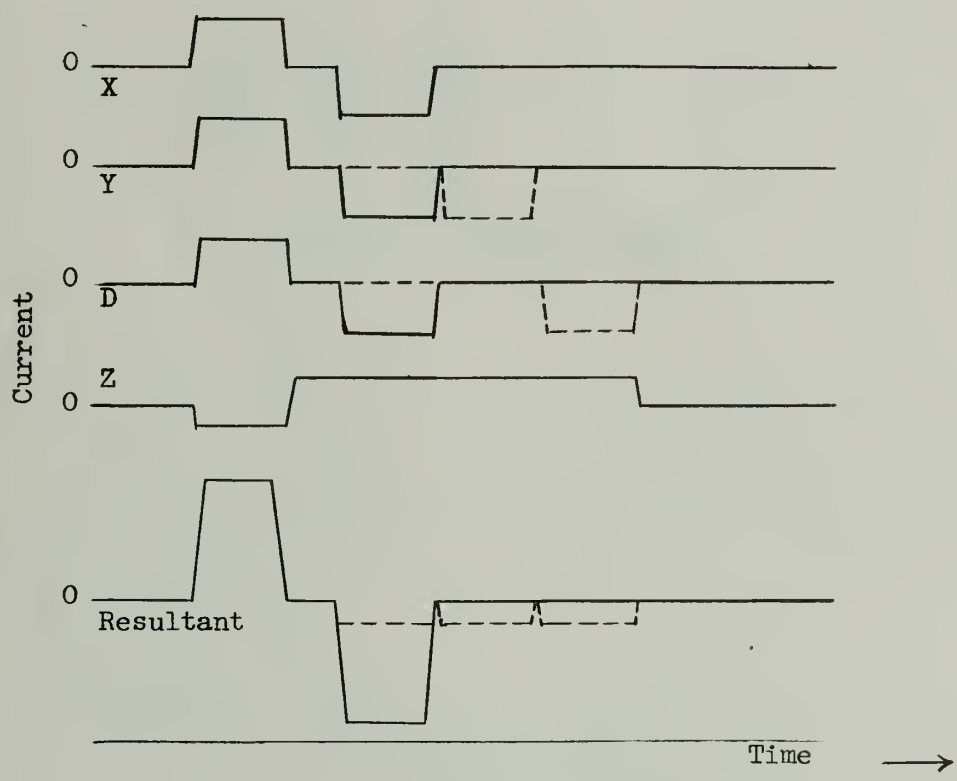

Figure 3: 5:1 Selection Ratio

1. Minnick and Ashenhurst, J. Appl. Physics, 26:575 (1955).
2. National Bureau of Standards Report, Program on Computer Components, October, 1954-March 1955.

that one winding from each set passes through the selected core and that no other core is threaded by more than one of these windings. The Z winding carries a current -I/2 during the "read" pulse and the chosen X, Y and D windings carry a current I. As can be seen from Figure 3 the resultant current through the selected core is 5/2 I, while the currents in other cores are 0, I/2 or -I/2. Thus the selection ratio is 5:1. When the selection ratio is higher, then the net driving currents are larger and the turnover time is shorter.

A somewhat different way of overcoming the current limitation is the "word-arrangement" memory,[2,3] illustrated by Figure 4 and Figure 5. In this

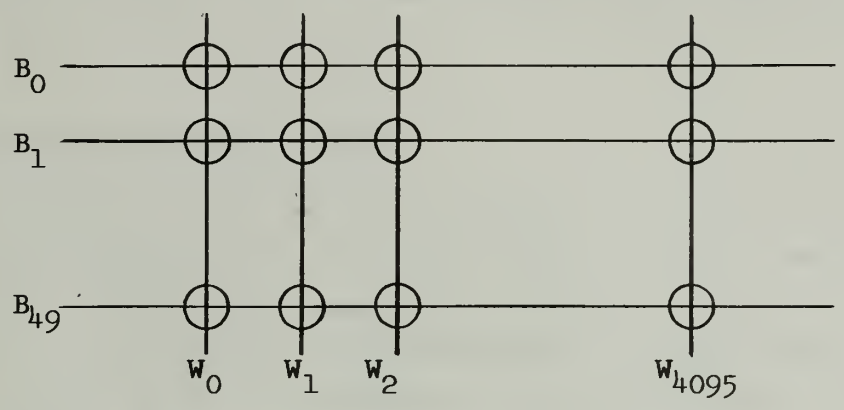

Figure 4. Word Arrangement

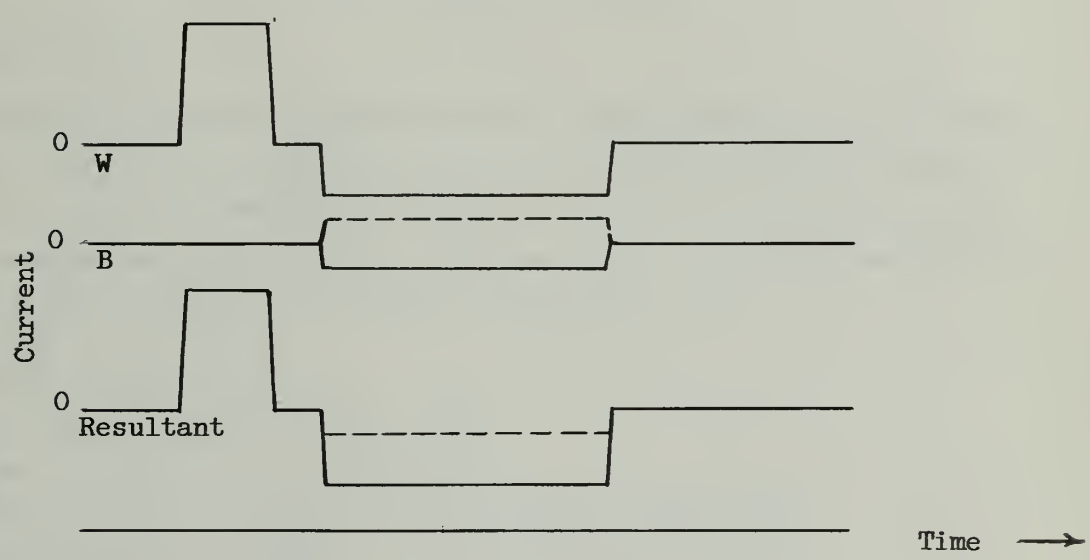

Figure 5. Word-Arrangement Pulses

2. See footnote on page 2.

3. J. M. Wier, A Dynamic Magnetic Core Memory, Report 54, Digital Computer Laboratory, University of Illinois, January, 1953.

arrangement one winding (marked W) passes through cores representing all the bits of a single word. In reading information from the memory the current through the appropriate W winding is not limited by any selection ratio. In rewriting the selection ratio with the waveforms shown would be 3:1.

Many variations of these arrangements are possible and with each of them the reduction in time is accomplished at the expense of more driving equipment, higher power, and in some cases more complex wiring of the memory cores. The most promising of the memories studied so far is the "word-arrangement" memory. Provided rather serious problems of current regulation and heat dissipation can be overcome a cycle-time of two to three microseconds seems possible.

Switching Properties of Magnetic Cores

In designing circuits involving storage cores or switch cores it is usual to use time-average values of output voltage, effective magnetizing resistance, etc. Actually these quantities vary widely during a cycle even with constant switching current. Some experiments are being carried out in an attempt to obtain a better approximation to actual properties of ferrite cores which is still simple enough to use in design problems.

Eccles-Jordan Flipflops

A study has been made of Eccles-Jordan type flipflops to find a set of circuit constants which would meet a set of tolerance conditions using the SB-100 surface barrier transistors. A program was written for Illiac to do this. This program was reported on at the Association for Computing Machinery in August, 1956.[4] The restrictions which were imposed were:

1) resistor tolerance ±2%,
2) power supply voltage tolerance ±3%,
3) nominal positive supply voltage 25v,
4) minimum collector voltage 0.1v (to prevent saturation),
5) minimum binary signal 2v,
6) SB-100 transistors, but no diodes,

4. G. H. Leichner, Report 72, Digital Computer Laboratory, September, 1956.

7) signal output load up to 0.5 ma,

8) alpha range 0.92 to 0.95 in one series of tests,

9) maximum collector voltage 20v,
maximum collector dissipation 30mw,
maximum collector current 5 ma.

With all of these restrictions it is believed that a design does not exist. However, if the maximum collector current or the maximum collector dissipation is increased a design could be found. Figure 6 shows a plot illustrating these things. Similarly if α could be restricted to 0.95 to 0.98 a design could be found.

These remarks provide an example of using the Illiac to find designs of these relatively straight-forward circuits.

The NOT circuit has been studied from an experimental standpoint using the surface barrier transistors. This is very similar to the flipflop problem, of course.

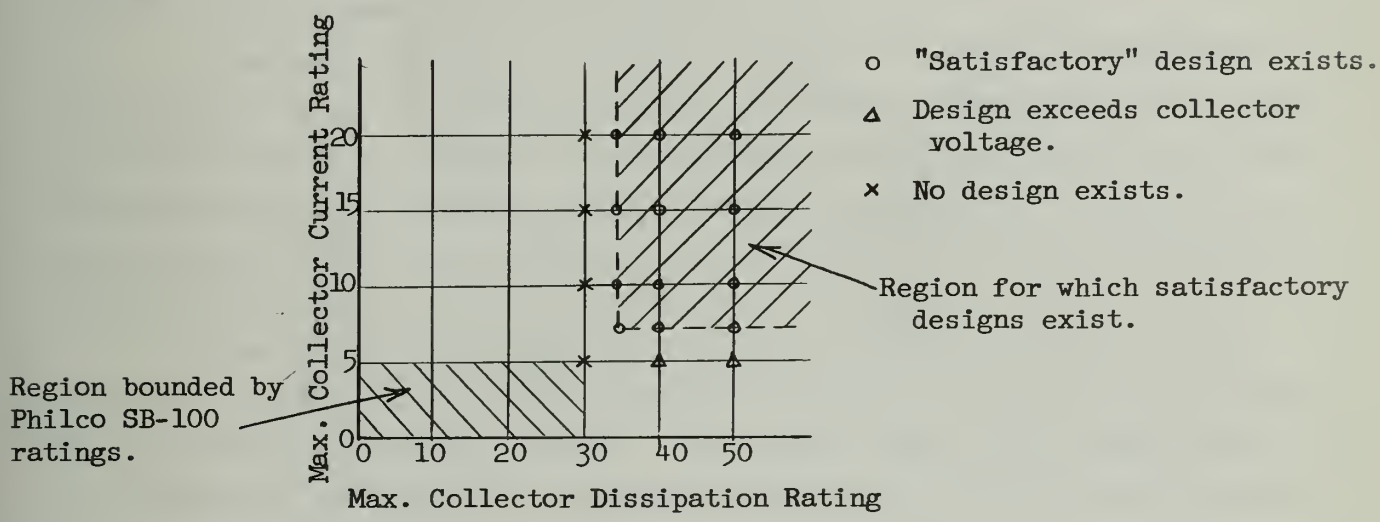

Figure 6. Region of Possible Flipflop Designs

Test Equipment for Fast Circuits

A number of units of test equipment have been assembled and tested which can be used to observe the operation of dc coupled circuits. A listing of these units follows.

EFP-60 Pulser. Characteristics:

Output pulse	+1v into 93 ohm cable at +150v level 50 mμs duration with rise time less than 8 mμs
Synch. pulse	separate output +0.5v into 93 ohm cable at ground level

The circuit uses an EFP-60 with plate to cathode feedback. The free dynode is used as the output terminal and a full 6J6 cathode follower provides a separate synchronization pulse output. Degenerative dc feedback is applied to the grid of the EFP-60 to increase the amplitude stability. The circuit is constructed in a small brass chassis with very short leads. The supply voltages required are the same as the amplifier to be described later.

Relay Pulser. A pulser using a Western Electric 275C mercury wetted relay was constructed. The duration of the pulse is determined by the length of coaxial cable used, and the repetition rate is 100 cps maximum. Pulses up to 10v have been formed with rise times less than 4 mμs.

A second relay pulser was built in which the relay was disassembled and mounted in a coaxial structure. This provided a better match to the lines since the relay as originally built by Western Electric has leads inside about two inches long. No decrease in rise time was observed with the second pulser but this was probably due to the 150 feet of RG-62/U cable which is necessary to delay the pulse to allow for the start of the sweep.

A low loss large diameter coaxial cable with $Z_o = 47\Omega$ was built to permit the fastest possible pulse from the relay pulsers even though such rise times cannot be observed at present. This coaxial cable may be used directly with the second relay pulser or with the first one with suitable modification of the matching network.

Display Equipment. In order to be able to observe the waveforms of fast transistor circuitry a wide band distributed amplifier was built using four EFP-60's.

Characteristics:	Gain	10 output not terminated
		5 output matched
	Rise Time	8 mμs
	Output	positive 10v maximum
		negative 20v maximum

The "delay lines" consist of 10 foot sections of RG-62/U cable with matching sections at each tube connection. DC feedback is applied to each tube to stabilize the current and, therefore, to a first order the gain of the amplifier.

A cathode follower using a 6BC4 triode, g_m = 10,000, with a gain of one-half was also constructed to drive the amplifier. The input capacity of this unit is 10.5 uuf direct and 6.5 μμf with a 2:1 attenuator. Series peaking is employed in the input to the cathode follower so an over-all rise time of 8 mps is preserved for the amplifier with cathode follower direct, and 6 mμs with the 2:1 attenuator is obtained.

Boolean Studies on Speed-Independent Circuits

A. Since speed-independent distributive circuits may be completely characterized by an initial state and a set of Boolean functions describing the nodal behavior, an investigation has begun to make possible the synthesis of the functions producing a circuit with prescribed behavior. The process of synthesis will be programmed for the Illiac to provide a useful tool for the circuit designer.

The development is through lattice theory and is begun by showing that the set of signals in a circuit completely characterizes a C-state diagram which is distributive. In general a speed-independent circuit may either cycle or reach equilibrium. In the latter case the partially ordered set of signals is finite while in the former it is countably infinite. However, a cycling circuit will eventually repeat (i.e., the C-state lattice will have a repetitive structure) so that the partially ordered set may be written in a finite manner by listing the coverings by congruences. At present methods of characterizing this partially ordered set are being studied with respect to ease of interpretation by a digital computer program.

B. The present library program (Q - 3) used for analyzing complete circuits for speed independence will be replaced by a more useful and more complete program. The new program will have the following characteristics:

(1) up to 78 nodes will be allowed;

(2) a cycling detection test will be provided;

(3) auxiliary equations not corresponding to nodes may be employed;

(4) a state may be designated as disallowed and a stop will occur if this state is attained;

(5) output indicating semimodular, distributive or totally sequential circuits will be more completely indicated.

The program will make use of the magnetic drum, incorporating a number of checks such as sum checks and overwriting tests. The compiler is now almost complete.

Relative Memory Sizes. Sorting

One of the important problems arising in connection with relative sizes of fast and slow memories is the sorting problem. A proper solution to this problem will affect design considerations. We consider here a method which minimizes accesses to the slow speed store.

Consider a random access memory (called core memory) and a serial memory (called drum memory). Let N_p words to be sorted be held initially on the drum and suppose that N is the number of words which, held in the core memory, can be correctly sorted into relative order among themselves without additional storage space.

A. Separate the words to be sorted into p N-word blocks N_1, N_2, ... , N_p in any manner (preumably as they occur), read N_1 into the core memory and mesh it in blocks of 1, 2, ... , N/2. Store the sorted block N_1 back on the drum and repeat for N_2, ... , N_p.

B. Next divide each of the sorted blocks N_i into k equal blocks N_{i1}, N_{i2}, ... , N_{ik} each of size N/k where N_{i1} are the N/k <u>largest</u> elements of block i (in correct order), N_{i2} are the N/k <u>next largest</u> elements, etc.

Read N_{i1}, i = 1, 2, ... , p into the core store, marking the last word of each block in some way. Mesh these into correct order by successive meshes of pairs of blocks, pairs of results, etc. This new sequence Q_1, correctly sorted, has the property that if X_1 is the first element in Q_1 which was a

last element of any block N_{i1}, then X_1 and all larger elements are sorted into their final order, for each is larger than any element in N_{ij} for $j \geq 2$ since each is larger than the last (smallest) element in N_{i1}. This in turn is larger than any element in N_{ij} for $j \geq 2$ because N_i is in its correct order. Thus the elements X_i and above may be stored away on the drum in their <u>final form</u>.

If X_1 was the last element of $N_{i_1 1}$, read in block $N_{i_1 2}$ and also, if space permits, read in a number of other blocks N_{j2} which are going to run out soon (i.e., whose last element in the core memory is near X_1). The resulting blocks are first meshed among themselves and then meshed with the previous list beginning with the word after X_1. This new ordered list also has the property that the elements beginning with the last element of the first block N_{ij} to run out and running up to the maximum are correctly ordered in their final form and may be stored on the drum. This process is continued until the meshing of N_1, N_2, ... N_p has been completed.

This process, if drum transfers are disregarded, is an N log N method. It requires 2 drum reads and 2 drum writes per number. If the average waiting time for one block N_{ij} is assumed to be 8 to 24 ms (the time to read 1,000 to 3,000 words), this system has the advantage that if k is correctly chosen we read about k/2 blocks, thus reducing the waiting time to get the first two blocks out to from 8/(k/4) to 24/(k/4) milliseconds. After that the first steps in the meshing process can continue during waiting time for the drum.

The problem is to choose the optimum k for given N_p. This should be done so that the average amount of sorted data written on the drum at each writing period (B) is about half the data since meshing is most efficient if blocks have equal size. A Monte Carlo model has been constructed for experimenting rapidly with random numbers on the Illiac to test the efficiency and to develop empirical rules for finding k.

The method applies to meshing N_q numbers out of a set of N_p numbers, so another possibility is to do the meshing in several stages. The results of the experiments will be used to decide whether or not this is useful.

<u>Register Number Study</u>

The variations of the multiplication-addition operation, $a \cdot b + c$, suggested by several numerical computations, have been summarized into the following 3 cases:

(1) (a) and (b) vary; (c) is fixed;

(2) (a) and (b) are fixed; (c) varies;

(3) (a) and (c) are fixed; (b) varies;

where (a) denotes the address of a, etc. Examples of calculations which might use these variations of $a \cdot b + c$ and orders for representing them are as follows.

A. Scalar Multiplication: $\sum_k a_{ik} b_{kj}$. The numerical computation would be carried out as: ----- $a_{13} b_{31} + \left[a_{12} b_{21} + \left[a_{11} b_{11} + 0\right]\right]$. Here (a) and (b) vary; (c) is fixed. The orders for carrying out this calculation would be:

51	(n)			
MS_i	(m)	:	(1)	$\left[Q \cdot m + 2^{-39} A\right] + S_1$
			(2)	$A \longrightarrow (S_i)$
			(3)	$Q \longrightarrow (A)$

The address (m) specified the multiplicand.

B. Polynomial Evaluation: $\sum_{i=0}^{n} a_i x^{n-i}$. The numerical computation would be carried out as: ----- $x \left[x \left[xa_0 + a_1\right] + a_2\right] + a_3$ ----- . Here (a) and (b) are fixed; (c) varies. The order for carrying out this calculation would be:

NS_i	(n)	:	(1)	$\left[Q \cdot S_1 + 2^{-39} A\right] + n$
			(2)	$A \longrightarrow (S_i)$
			(3)	$Q \longrightarrow (A)$
			(4)	reset Q

The address (n) specifies the addend.

C. Simpsons Integration: $\int_a^b f(x)\, dx$. The numerical computation would be carried out as: $\frac{1}{b-a} \int_a^b f(x)\, dx = \frac{1}{3n} \left[f_0 + 4f_1 + 2f_2 + 4f_3 + \ldots + 4f_{n-1} + f_n\right]$. Here (a) and (c) are fixed; (b) varies. The order for carrying out this calculation would be:

PS_i	(n)	:	(1)	$S_2 \longrightarrow (Q)$
			(2)	$\left[Q \cdot n + 2^{-39} A\right] + S_1$
			(3)	$A \longrightarrow (S_i)$
			(4)	$Q \longrightarrow (A)$

The address (n) specified the multiplicand.

It should be noted that:

(1) The general notation for the above orders would be MV (n), NV (n) and PV (n), thus permitting full use of the variation character. When $V = S_i$ the multiplication is assumed to be carried out on the algebraic values of the operands, and the S_i specified the particular S register to which the most significant part of $a \cdot b + c$ is transferred.

(2) If the addition is suppressed (denoted by $^{-}$), the operation $a \cdot b + c$ becomes $a \cdot b$. In general then, $\overline{MV}$ (n) may include any of the ILLIAC multiplication orders. A particularly useful result of this innovation is the order $\overline{PV}$ (S_2) which, if $x = S_2$, forms the product x^2, while $\overline{P}S_2$ (S_2) would replace x by x^2 in (S_2).

(3) Although the function of these orders is similar to that of 2 - address and 3 - address orders, the single address structure of the ILLIAC order code is still maintained. Each order specified one address; however, the address of the supporting S register involved is implicitly specified by the order type. That is, M implies that the contents of a given S register, say (S_1), will be added to the product; N implies that the multiplicand will be taken from a given S register, say (S_2), etc. The innovation of introducing a third address, i.e., substituting S_i for V, has been discussed before.

(4) A fourth case, viz., (a) and(c) are variable, (b) is fixed can be included in the case C by the following order pair (assuming A = 0 and $b = S_2$).

LS_1	(c)
PV	(a)

A pseudo 3 - address order may also be considered for addition. Such an order might be

US_i (n) :	(1)	$S_1 \longrightarrow (A)$
	(2)	$A + n$
	(3)	$A \longrightarrow (S_i)$

where here, again, the address S_1 is implicitly specified by the order type U.

The following results were obtained after programming Library Routine S3, Logarithm, for PAC-1-2-3. A new order $\overline{PV}$ (n) was used in this routine.

	W*	OA	IA	TS
Illiac	14	7 + 7 (39) + 2m	6 + 7 (39) + 3m	3
PAC - 1	$13\frac{1}{2}$	5 + 3 (39) + 2m	6 + 6 (39) + 3m	2
PAC - 2	13	1 + 2m	6 + 6 (39) + 3m	1
PAC - 3	13	1	6 + 6 (39) + 3m	0

(1) m is defined by:

$$\log_2 x = \log_2 2^{-m} + \log_2 W; \; 1/2 \leq W < 1$$

(2) The quantity (39) denotes the number of passes through the loop determining $\log_2 W$.

It will be noted that the value of IA is almost constant although OA is reduced to its minimum. This is because the sequence of numerical operations of the corresponding Illiac program was followed. The orders of the PAC codes chosen, which followed the Illiac pattern, did not lend themselves to any combinations arising in the logarithm routine. This indicates a need to investigate in the direction of significant departure from Illiac methods.

* W = number of words

OA = accesses for operands

IA = accesses for instructions

TS = temporary storage

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

A final description is being prepared of the program for solving systems of simultaneous linear algebraic equations using the magnetic drum. The program will solve about 140 equations by the elimination method.

Library routines N-5 and N-6 which read fractions and integers from tape and put them on the drum are being combined into one routine with the following characteristics:

(1) Sum checks are provided.

(2) A word count of the number of words recorded on the drum is obtained.

(3) Integers and fractions may be arranged as desired on the tape.

(4) First drum locations of sequences, if desired, may be determined from the tape.

PART III

MATHEMATICAL ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794)

A study is being made of the Einstein field equations for the gravitational field due to a plane symmetric distribution of a perfect fluid undergoing adiabatic motion. It is hoped that the results previously obtained for isentropic motions may be generalized to this case. A co-moving coordinate system is used. In this coordinate system the metric tensor involves only three functions. However because the motion is not isentropic the stress energy tensor is not directly given in terms of these three dependent variables. Nevertheless by considering the pressure as a prescribed function of the coordinates one may obtain equations for the components of the metric tensor. These equations are being studied in special cases. It is planned to solve them numerically if analytic solutions cannot be obtained.

Two new techniques for the numerical integration of systems of ordinary first-order differential equations with given initial values have been investigated. Work has been begun on further investigation of the numerical solution of Sturm-Liouville problems. This will supplement the work done during the last two years.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During September specifications were presented for 7 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 868. Numbers followed by T are for theses.

868 Midwestern Universities Research Association. The Motion of a Particle in a High Energy Accelerator. This problem involves the solution of four coupled nonlinear differential equations by means of the Runge-Kutta method.

869 Psychology. Analysis of Q-Sort Descriptions of Abnormal Children. Factor analyses and other statistical studies will be made.

870 Electrical Engineering. Radiation Field Produced by a Slotted Wave Guide. The radiation field excited by an incident wave on a slotted wave guide is solved using a number of parameters.

871 T Speech Department. Relationships between Vocal Responses to Delayed Auditory Feedback and Certain Personality Measures. Disturbances in speech are produced by playing back the speech after it has been delayed slightly. The amount of disturbance produced in this way is correlated with various speech measures and personality measures.

872 University of Michigan. Selection of Medical Students. Various data collected on medical students at the University of Michigan are to be analyzed statistically.

873 Physics. Relativistic Two-Body Dynamics Problem. This program is designed to calculate energies and angles resulting from bombarding a particle of mass m_2 with a projectile particle of mass m_1. The formulas computed by the program carry out the transformations into a center of mass coordinate system.

874 Structural Research. Analysis of Flat Slabs and 2-Way Slabs. The problem is a series of analyses of flat slabs and 2-way slabs under various loading combinations. The problems to be solved by the Illiac are algebraic, linear simultaneous equations which are obtained by the method of finite differences.

Table I shows distribution of machine time for the month of September.

TABLE I

Regular Maintenance	27:57
Unscheduled Maintenance	18:15
Drum Engineering	35:33
R.A.R.	4:19
Leapfrog	48:39
Wasted	:01
Use by Departments	
Computer Group	5:00
Physics	20:53
Control Systems Lab.	7:38
Structural Research	2:04
Struct. Res. (DA-11-02-ORD1980)	:16
Struct. Res. (AF 24994)	:29
Psychology	11:55
Psychology (MD 620)	6:04
Electrical Engineering	3:27
Elec. Eng. (AF 3220)	1:21
Chemistry	49:01
Agriculture	6:30
MURA	165:24
Ill. Dept. of Public Welfare (Coan)	10:44
Ill. Dept. of Public Welfare (Hurley)	5:25
University of Michigan	1:42
Demonstrations	1:25
Miscellaneous	29:45
Total	463:47

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for September.

TABLE III

Reader Errors	11
Punch Errors	0
Control Errors	2
Memory Errors	1
Drum Errors	4
Scope Errors	1
2L type Error (leapfrog)	4
Unknown	5
Total	28

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
9/4/56	20:00	:00	0		00	1:10	0
9/5/56	19:52	:08	1	(1) Coupling on Reader "B" broken	00	1:22	0
9/6/56	19:59	:01	1	(1) Tape tore in reader "B"	00	1:32	0
9/7/56	20:00	:00	0		00	1:29	0
9/10/56	13:14	6:46	2	(1) Memory position 2^{-12} error (2) Open filament in V-18 reg. selection chassis	00	1:08	0
9/11/56	20:00	:00	0		00	:56	0
9/12/56	19:50	:10	1	(1) Drum error. Drum routines would not read back to Illiac without error.	00	1:22	0
9/13/56	19:59	:01	1	(1) Film jammed in cassette	00	1:05	0
9/14/56	20:00	:00	0		00	1:02	0
9/17/56	18:44	1:16	2	(1) Cross talk on drum (2) Light out on reader "B"	00	:58	0
9/18/56	19:58	:02	2	(1) Unknown (2) Unknown	00	1:11	0
9/19/56	13:33	6:27	3	(1) Unknown (2) Unknown (3) 2L type failure, Leapfrog	00	:55	1
9/20/56	17:45	2:15	6	(1) 2L type failure, Leapfrog (2) 2L type failure, Leapfrog (3) Dirt on sprocket hole of reader "K" (4) Reader "K" error (5) 2L type failure, Leapfrog (6) Unknown	00	3:09	3
9/21/56	19:59	:01	1	(1) Reader "K" error	00	2:31	0
9/24/56	19:18	:42	5	(1) Reader "K" error (2) Reader "K" error (3) Reader "K" error	00	1:44	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
				(4) Control (5) Reader "K" error			
9/25/56	20:00	:00	0		00	1:01	0
9/26/56	19:58	:02	2	(1) Reader "B" error, voltage setting too low	00	1:01	0
				(2) Drum Failure	00	1:36	0
9/27/56	19:59	:01	1	(1) Drum error	00	2:41	0
9/28/56	20:00	:00	0		00	3:15	0
TOTALS	362:08	17:52	28		00	28:27	4

Comments on the Illiac and Related Equipment

A new photoelectric tape reader control logic was reviewed in anticipation of its installation in the machine. This logic allows the tape brake to be applied immediately after the character is read. The tape is permitted to stop either on the sprocket hole of the character read last or on the sprocket hole of the next character to be read or anywhere inbetween. In the present tape reader control the last sprocket hole had to be passed by before braking could occur. The extra stopping time effectively allowed the reader is that corresponding to the time from the beginning to the end of a sprocket hole.

The regular maintenance of the drum memory is now arranged so that tubes are checked about every three months as compared to every six months as previously planned. During the month in the regular running of drum test codes a total of 23 errors occurred during 33 hours of test codes. A new test code due to Mr. Carter has been more helpful than previous ones in locating intermittent playback errors. The 6AU6 preamplifier tube has been replaced in about one-half of the units by a type 6136.

The new photoelectric tape comparer was completed by the shop and put into regular use in the Teletype Room. A similar high-speed reperforator unit for the Teletype Room is being built in the shop.

Reports and Seminars

Reports

Laboratory Report No. 72, "Designing Computer Circuits with a Computer," by Gene H. Leichner, September 17, 1956.

Seminars

"An Introduction to Error Detecting and Correction Codes, by G. A. Metze, September 25, 1956.

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UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

October 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computing Centre and Department of Physics.

A Proposal for Design of Arithmetic Unit

Introduction

Recently, a number of proposals for increasing the speed of an arithmetic unit have been suggested. These include:

a) Use of a carry completion circuit to sense the end of the longest carry sequence, during an addition, regardless of when and where it occurs.[1]

b) Use of a carry register for storage of carries during multiplication,[2,3] eliminating the necessity for completion of carry sequences during intermediate steps.

c) Sensing of multiplier digits in such a way as to reduce the number of additions required per multiplication.

During October, an investigation was begun to determine the structure of a fixed-point binary arithmetic unit embodying the above design features. The results of the investigation indicate that considerable gains in speed of operation can be made with a relatively small increase in complexity of hardware of the arithmetic unit. Furthermore, it appears that additional speed of operation can be gained only by a relatively great increase in the amount of hardware.

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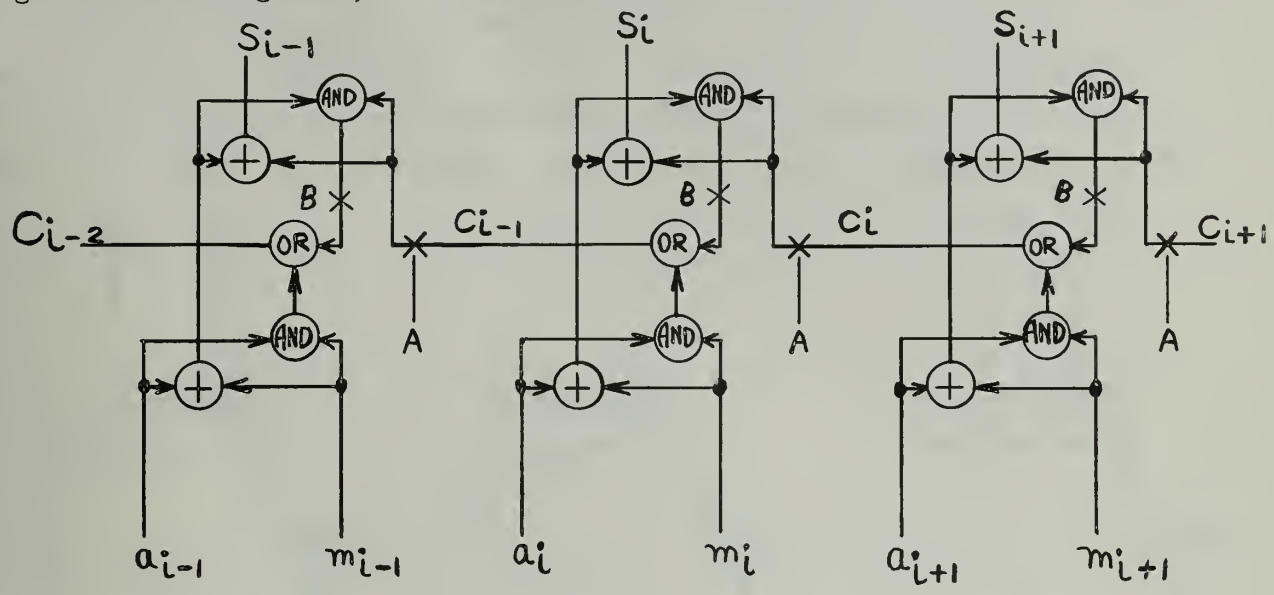
1. B. Gilchrist, J. H. Pomerene, and S. Y Wong; "Fast Carry Logic for Digital Computers," IRE Trans. on Electronic Computers, vol. EC-4, no. 4, pp. 133-136, December 1955.

2. G. Estrin, B. Gilchrist, and J. H. Pomerene; "A Note on High-Speed Digital Multiplication," IRE Trans. on Electronic Computers, vol. EC-5, no. 3, p. 140, September 1956.

3. J. E. Robertson; "Preliminary Design of an Arithmetic Unit for Use with a Self-Checking Binary Parallel Digital Computer," University of Illinois Digital Computer Laboratory Internal Report #19, June 1950.

Adder Structure

The structure of a conventional binary adder is indicated in block diagram form in Figure 1, in which the symbols represent circuits whose opera-



$$s_i = a_i \oplus m_i \oplus c_i$$

$$c_{i-1} = (a_i \oplus m_i)c_i \vee a_i m_i$$

Figure 1. Conventional Adder

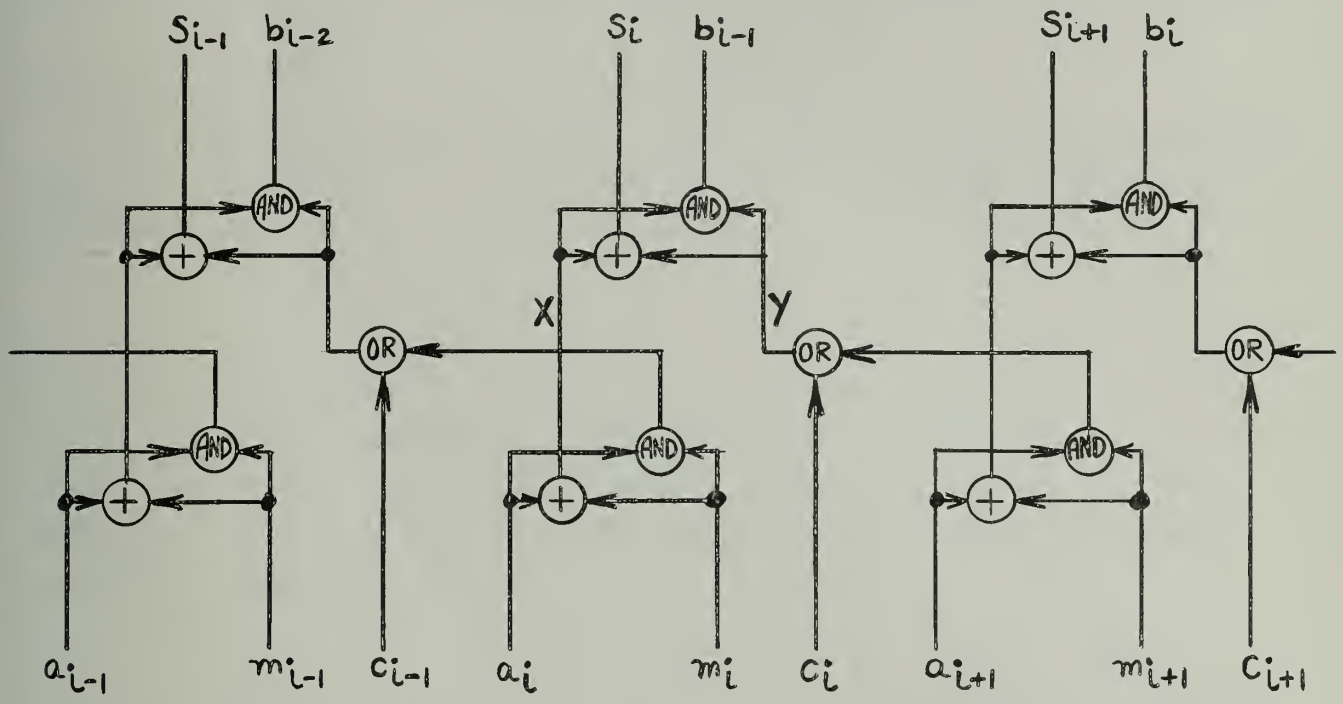
tions are summarized in the following table:

x	y	x → AND ← y, x·y	x → OR ← y, x y	x → + ← y, x+y
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

If we employ Illiac terminology, the digits a_i $(i = 0,\ldots 39)$ represent binary digits of the accumulator register A, the m_i are digits of the number register R^3, the s_i are sum digits to be gated to $\overline{A}$, and the c_i are carry signals

internal to the adder. The ultimate speed of the conventional adder is limited by the fact that sufficient time must be allotted for the carry to propagate from the least significant to the most significant digital position.

If register storage for carries is provided, the carry chain can be broken either at points A or points B of Figure 1. For reasons given in the next section, breaks at point B are preferable, leading to the logical structure of Figure 2. In Figure 2, the digits b_i would be gated to a temporary carry register



$$s_i = a_i \oplus m_i \oplus \left[a_{i+1}\, m_{i+1} \vee c_i\right] \qquad b_{i-1} = \left[a_i \oplus m_i\right] \cdot \left[a_i + m_{i+1} \vee c_i\right]$$

Figure 2. Proposed "Adder" Structure

$\overline{C}$ and digits c_i are held in the carry register C. The logical structure of Figure 2 together with the registers A, $\overline{A}$, C, $\overline{C}$, and R^3 and suitable interconnecting gates, is sufficient for sequences of additions and subtractions, including sequences required for multiplication. The true sum at any given instant of time would be found by adding the contents of A and C, or alternatively of $\overline{A}$ and $\overline{C}$. The process of finding the true sum from the contents of accumulator and carry registers will be called carry assimilation.

Carry Assimilation

An important consequence of selecting points B of Figure 1 as the break points in the carry chain is that the digits s_i and b_{i-1} of the ith digital position cannot simultaneously be ones. This readily follows if we let

$$x = a_i \oplus m_i \quad \text{and} \quad y = a_{i+1}\, m_{i+1} \vee c_i$$

and note that $$s_i = x \oplus y, \qquad b_{i-1} = x \cdot y$$

and note further that $$s_i \cdot b_{i-1} = (x \oplus y) \cdot (x \cdot y) = 0.$$

For carry assimilation, we first assume that a full adder of the structure of Figure 1 is required, with inputs s_i and b_i, with internal carry d_i, and with sum digits a_i. The equations for carry assimilation are then

$$a_i = s_i \oplus b_i \oplus d_i \qquad\qquad d_{i-1} = (b_i \oplus d_i)s_i \vee b_i \cdot d_i$$

We now show that $b_i \cdot d_i = 0$ follows from $s_i \cdot b_{i-1} = 0$, by induction on i. For $i = 39$, $d_{39} = 0$, therefore $b_{39}d_{39} = 0$. The induction hypothesis is $b_i \cdot d_i = 0$. If $d_{i-1} = 1$, then s_i must equal 1, implying that $b_{i-1} = 0$ and $b_{i-1}d_{i-1} = 0$. If $b_{i-1} = 1$, then $s_i = 0$ and $d_{i-1} = 0$. The carry assimilation equations can therefore be simplified to

$$a_i = s_i \oplus (b_i \vee d_i) \qquad d_{i-1} = s_i \cdot (b_i \vee d_i)$$

Thus the circuitry for carry assimilation is approximately half as complicated as the circuitry for a conventional adder.

The remarks of the preceding paragraph are based upon use of a conventional carry chain in the carry assimilation circuitry, rather than carry completion circuitry. It is proposed that the carry assimilation circuits be designed with two carry completion signals, one for the longest carry sequence and one for the sign digit. It is also proposed that the carry assimilation circuits should be attached to $\overline{A}$ and $\overline{C}$, with the assimilated sum gated to A when required.

Alternatively, carry assimilation could be performed by converting the structure of Figure 2 to that of Figure 1 by suitable switching circuits. It appears that switching circuits for such conversions are as complicated as those for separate carry assimilations described in the preceding paragraphs,

and have the further disadvantage of increasing the number of circuits through which the carry must propagate.

For maximum speed of operation, carry assimilation sould be performed only when absolutely necessary; namely, when the number in A is to be transferred elsewhere; or in parallel with some other operation; e.g., reading from core storage. For sign conditional operations, such as those which occur in division and sign conditional jumps, it is proposed that the sign digit carry completion signal be used to indicate that the sign has been correctly determined.

Multiplication with Negative Multiplicand

Multiplication can be sequenced as a series of conditional additions and shifts and requires the "adder" structure of Figure 2 with registers R^3, A, $\bar{A}$, C, $\bar{C}$, Q, $\bar{Q}$, with right shifting facilities from $\bar{A}$ to A, $\bar{C}$ to C, and $\bar{Q}$ to Q. The Illiac multiplication for negative multiplicand requires the insertion of the sign digit of A during the right shift; the sign digit is determined from signs of multiplicand, partial product, and their sum in $\bar{A}$. In the proposed arithmetic unit, determination of the sign of the sum is time-consuming and is to be avoided. A valid procedure is to insert the equivalent of the two's complement of the multiplier. The complement of the multiplier is inserted digitwise into the most significant digits of A as the right shifts are executed; this complement is easily determined if serial sensing of the multiplier digits, least significant digit first, is employed.

Minimization of Additions during Multiplication

With the complementing circuit located between the multiplicand register R^3 and the adder, it is possible to both add and subtract the multiplicand from the partial product in the accumulator A. A sequence of n ones in the multiplier, such as $2^{-(i+1)} + 2^{-(i+2)} + 2^{-(i+3)} + \ldots + 2^{-(1+n)}$, is equivalent to $2^{-i} - 2^{-(i+n)}$. Thus n additions can be replaced by one addition and one subtraction. The method requires the sensing of two multiplier digits and a mode flipflop indicating whether addition or subtraction is to be performed, and can be described by the following rules:

Multiplier digits

	q_{38}	q_{39}	
+ mode	0	0	Shift right
	0	1	Add -icand and shift right
	1	0	Shift right
	1	1	Change mode to -, subtract -icand, and shift right
- mode	0	0	Change mode to +, add -icand and shift right
	0	1	Shift right
	1	0	Subtract -icand and shift right
	1	1	Shift right

Reduction of Number of Shifts during Multiplication

One feature of the addition minimizing method of multiplication should be noted. If an addition or subtraction is performed, the next step is a shift. For example if the + 1 1 state resulted in a subtraction, the next state would be either - 0 1 or - 1 1 since q_{38} replaces q_{39} for the next step. Neither of these states requires an addition or subtraction; similarly, any other state requiring use of the adder is followed by a state which requires only a shift.

It is therefore proposed that a right shift of two places be employed for multiplication. The result might be considered a modified base 4 multiplication method, and requires that the first and second multiples of the multiplicand be available to the complementing circuit as indicated in Figure 3.

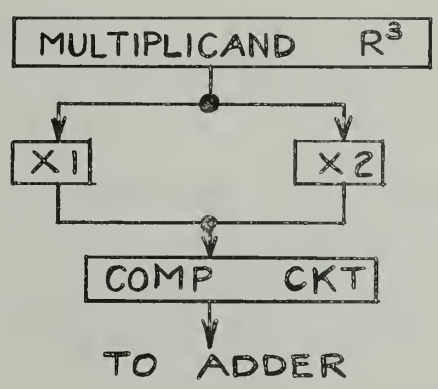


Figure 3. Multiplicand Sensing Circuit

The second multiple is easily obtained by sensing each digit one digital position to the left of the one normally sensed. The adder and registers $\overline{A}$ and $\overline{C}$ would have to be extended one digital position to the left.

Negative Multiplier Correction

The method of multiplication of a multiplicand x by a multiplier y is as follows.[4] If y is positive the product xy is formed; if y is negative, the product (-x)(-y) is formed. The method requires that the sensing of the multiplier digits be complicated so that the digits are interpreted as those of the two's complement of the multiplier if the multiplier is negative. This proposal is compatible with the requirements for digitwise insertion of the two's complement of the multiplier into the most significant digits of A during the right shift for negative multiplicand.

Division

Division presents a special problem in that at each step, the sign of the difference (or sum) of the partial remainder in A and the divisor in R^3 must be found. For a restoring division, the sign of the difference (or sum) is sensed to determine whether the difference (or sum) is shifted or whether the old partial remainder is shifted to form a new partial remainder. For non-restoring division, the sign determines whether an addition or subtraction is to be performed during the next step. Thus it seems that a non-restoring division can be performed more rapidly, particularly since the carry assimilation to the sign digit can occur in parallel with the transfer with shift from $\overline{A}$ to A and $\overline{C}$ to C.

Summary of Characteristics

For multiplication, this proposed arithmetic unit has the following characteristics:

1) The number of carry propagations is minimized,
2) the number of additions (or subtractions) is minimized,
3) the number of gating operations for shifts is half that required for a purely serial sensing of multiplier digits,

4. J. E. Robertson; "Two's Complement Multiplication in Binary Parallel Digital Computers," IRE Trans. on Electronic Computers, vol. EC-4, no. 3, pp. 118-119, September, 1955.

4) extra steps for corrections have been eliminated with the exception of the special case of a multiplier equal to -1.

It is felt that division time can be further reduced only by resorting to much more complicated and expensive techniques.

Proposals for Future Study

The previous sections present a broad outline of a proposed fixed point binary arithmetic unit. Many details are yet to be considered, such as:

1) Detailed design of multiplier digit sensing circuits,
2) investigation of properties of binary numbers for determination of average number of additions per multiplication and of average time required for sensing the sign through carry assimilation circuits.
3) circuit requirements for division with rounded quotient and for division with unrounded quotient and correct remainder,
4) treatment of the special case of a multiplier equal to -1.

Broader problems that remain include:

1) Imposing the requirement of speed independence on the design,
2) consideration of floating point operation.

Effects on speed and hardware requirements of variations from the proposed design should also be studied; for example, the removal of the requirement of carry completion signals in carry assimilation circuits.

Boolean Circuit Theory

General Asynchronous Circuits

New results in asynchronous circuit theory are being written up in a nearly completed report (Digital Computer Laboratory Report No. 75). In it the theory of asynchronous circuits was extended from the binary, or two-valued, to the multiple-valued case. The new material contained in the report is largely concerned with this extension, but several completely new theorems also appear in it. The following list summarizes the important new developments.

1) A new definition was set down for a circuit and a set of states. (2:1)
2) A new definition for an allowed sequence of states which is not an obvious extension of the binary case. (3:3)

3) Two new theorems describing the behavior of a general asynchronous circuit. (3:F) and (3:G)

4) A new definition for a pseudo final set of states. (3:17)

5) A new definition for a semi-modular circuit. (5:3)

6) A new proof that a semi-modular circuit is speed independent. (5:C)

Semi-Modular Circuits

A second report will use the concept of semi-modularity and will develop further the properties of the semi-modular class of speed independent circuits. As in the two-valued theory, a concept of a cumulative state can be introduced, and many of the earlier theorems in the two-valued case have their analogs in the more general theory. The definition of the length vector of an R sequence over the positive integers leads to a central theorem, to the development of uniqueness properties, and to the formation of a semi-modular lattice. The existence of this lattice is important since many of the later results of the two-valued circuits were derived from lattice properties and were independent of the assumptions of two-valued logic. Consequently these results can be expected to carry over into the new theory without much modification.

Illiac Circuit Analysis

The compiling routine for the revision and extension of Library Routine Q-3, Complete Circuit Analyzer (see Progress Report for September 1956) was completed and checked and the main program is about 55% complete in first draft form.

Sorting

Sorting is being studied for the new computer to decide what methods are best and what features of such a machine would speed up sorting. The method chosen for sorting depends on the number of data and their probable initial order. However, for most problems, block merging is probably the best method after equal sized ordered blocks, of say 4 to 30 items each, have been obtained. In merging R ordered blocks of data to form one large ordered block, the basic operation is to compare the k highest remaining items, one from each block, and transfer the winner to the next position of the merged block. This requires k-1 comparisons for the first winner, and, using previously obtained information, $\langle \log_2 k \rangle_+$ comparisons at most, for each succeeding winner. The items in any one block are

processed in serial order, but the time when a given item will become the highest remaining item of the block depends on the items of the other blocks.

Given a hierarchy of stores (including some or all of the following: fast access register, a core store, a drum store, and magnetic tape units) the fastest sorting procedure seems to be to merge successively in the fastest access store until an ordered block as large as possible has been obtained. This is moved to the second fastest store of the hierarchy, and the procedure is repeated. When the second store is nearly full of these medium-sized blocks, these are merged into one large-sized block which is transferred to the next store of the hierarchy. This process is continued until all the data are in blocks on tape, each block about the size of all the other stores combined. These blocks are merged during a sequence of tape passes, each pass involving reading by half of the tape units and writing by the other half. During a tape pass, the blocks consisting of the first block in each input tape are merged into one block which is written on the first output tape; the second blocks on all input tapes are merged and written onto the second output tape, etc., the output tapes being used in rotation.

Except for the initial tape pass during which large blocks are pre-sorted internally and placed on tape, it seems that neither merging nor any other <u>sorting method</u>* can take advantage of the facility of simultaneously reading from several tapes, or writing on several tapes at once, except for reducing start-stop times on tape. For 2k tape units, and C words in the core store, start-stop times can be estimated from the fact that a tape moves uninterruptedly while about $(\frac{C}{2k})$ words are read or written. If T is the word time for tape, the time for tape sorting is proportioned to $(\frac{T}{\log_2 k})$. At least 4 tape units are required. Speed can be doubled if it is possible to write on one tape while reading from another. Rewind time can be eliminated if it is possible to read in one direction and write in the other. If N is the number of items, and if F is the number of items that can be sorted internally, the number of tape passes for the entire data is $\log_k (\frac{N}{F})$. At present tape speeds, a one-word switchable buffer for each of tape-reading and tape-writing would certainly suffice unless time-sharing were considered to be an important possibility. In this case buffers large enough to allow one drum revolution time of free calculation would be very nice.

* For <u>filing</u> additional data into a sorted list already held on tapes, simultaneous reading and writing are useful.

Present tapes (about 1/4 ms per word) are so slow that not only is there plenty of time for merging the words while running the tapes at full speed, but the rate of pre-sorting the data into blocks of say 2^{15} words would probably average less per word than the time to read from tape. If faster tapes became available so that pre-sorting becomes an important part of sorting time, it would be possible to rearrange the order of calculation in order to do most of the tape merging of early blocks during the pre-sorting of later ones.

For drum-and-core-store sorts the problem is more complicated than for tape sorts. The word-time on the drum should be as near to the access time of the core store as possible, and if the times are nearly equal it should be possible to sort nearly as fast as with a large core store. However, if the number of words which can be read from the drum in one drum revolution is not small compared to the word-capacity of the core store, there is too little calculation to use all of the waiting time for the drum. If time-sharing is allowed, or if the core store is sufficiently large, random accesses can be eliminated and all blocks on the drum can be simultaneously merged.

The problem of sorting in the core store alone, if it is frequent enough, suggests the possibility of a special "merge" instruction, or two or three less specific instructions which, in combination, produce the same effect. The merge instruction would require 3 B-registers for a two-way merge and at least 2 registers in the arithmetic unit. The basic operation is to read one word from the sequence which yielded the latest low value (high value), compare with the word from the other sequence still held in the arithmetic unit, store the winner of this comparison in the next free location of the merged list, count on the B-registers of the winner' list and the merged list, and recycle unless one of the B-registers reached its final value.

A method of merging has been found which requires only 3N/2 storage locations.

Register Arrangement

A study is being made of a logical structure in which the function digits of an instruction refer to an auxiliary memory for decoding of the instruction while the operand is being obtained.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Faster Input Routines

A new logical design for the Illiac photoelectric reader provides possibilities for faster input routines provided that the inner repetitive loops of the routines can be made faster. Three new input routines with faster loops have been written.

Floating Address Routine and Drum Storage of Library Routines

The floating address routine is being speeded up and a program is being written for use with it which will pull library routines from the drum into the Williams memory when they are called for by special coding on the tape input of a program. A code like (P1) 372K, for example, will bring routine P1 from the drum and store it beginning at location 372 of the Williams memory.

Program Library

The following routines were added to the program library in October. Library Routine E6, which was placed in the auxiliary library, was prepared by Professor B. L. Hicks and Mrs. Rosemarie Stemmler of the Control Systems Laboratory.

X-3 (222) Constant-Listing Auxiliary. 21 Words. This routine is a modification of X-3 (90) which is now obsolete and works with the new Decimal Order Input, X-1 (218).

X-AL (223) Constant-Listing Auxiliary for Floating Decimal. 18 Words + Routine A-1. This replaces X-A1 (123) which is now obsolete.

L-6 (224) Solution of a Set of n Simultaneous Linear Algebraic Equations Using Magnetic Drum Storage. 162 Words. This is an open routine which uses the elimination method of Library Routine L-1. It contains some modifications to aid in keeping as much accuracy as possible. When an element of a row exceeds one-half, the elements are all scaled by the factor 4/10 rather than by 1/10. Also, before being placed in the triangular

matrix the elements are scaled up to make the largest element lie in the range $1/4 \leqslant x < 1/2$. Sum checks and drum transfer checks are also included. The maximum capacity is 143 equations.

E-6 (221) Integration over a Single Interval (Tabulated Values). 32 Words. This program of the auxiliary library computes an approximation to an integral when the argument is tabulated. The order of the integration process, and therefore its accuracy, is controlled by a parameter.

PART III

MATHEMATICAL ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794)

The problem of determining the shock wave formed when a given streakline is specified in a flow behind the shock and the flow ahead of the shock is uniform has been shown to be equivalent to integrating the partial differential equations.

$$
\begin{aligned}
\frac{\partial \xi_i}{\partial T} &= A_{ij}(\lambda, \mu, m)\left\{\frac{\partial \xi_j}{\partial s} - C_j(\lambda, \mu, m, c)\right\} \qquad i,j = 1,2 \\
\frac{\partial c}{\partial T} &= \frac{\gamma - 1}{2}\, c\, \frac{\partial \xi_1}{\partial T} \\
\frac{\partial m}{\partial T} &= -\frac{1}{m}\left(1 + \frac{\gamma - 1}{2} m^2\right)\frac{\partial \xi_1}{\partial T} - \frac{1}{c} \\
\frac{\partial \lambda}{\partial T} &= \cos\mu\, \frac{\partial \xi_2}{\partial s} \qquad (1) \\
\frac{\partial \alpha}{\partial T} &= \frac{\sin\mu}{\lambda}\, \frac{\partial \xi_2}{\partial s} \\
\mu &= \xi_2 - \alpha
\end{aligned}
$$

given $\xi_2(0,T)$ and the Rankine-Hugonoit equations which hold on the unknown shock $(T = 0)$.

The numerical procedure is as follows: Assume $m > 1$ behind the shock. To solve the problem numerically we replace the partial derivatives in (1) by simple forward differences on a mesh $(\Delta s, \Delta T)$. This first order difference system is locally stable if

$$\frac{\Delta s}{\Delta T} \geqslant \frac{\sin\mu + \sqrt{m^2 - 1}\,\cos\mu}{\lambda(1 - m^2\cos^2\mu)} \qquad (2)$$

and convergent if, in addition,

$$\lambda(1 - m^2\cos^2\mu) > 0. \qquad (3)$$

Now suppose the unknowns have been found for all points $(\nu\Delta s, \rho\Delta T)$ where $\nu + \rho < n$. To obtain the values for $\nu + \rho = n$ we proceed as follows:

(i) Guess the inclination of the shock at $(n\Delta s, 0)$, $\alpha^{(0)}(n,0)$. This together with the knowledge of the oncoming flow enables us to solve the Rankine-Hugoniot equations for $\xi_i^{(0)}(n,0)$.

(ii) Compute $\xi_i^{(0)}(0,n)$ via

$$\xi_i^{(0)}(\nu,\rho+1) = \xi_i^{(0)}(\nu,\rho) + \frac{\Delta T}{\Delta s} A_{ij}(\nu,\rho)\left\{\xi_j^{(0)}(\nu+1,\rho) - \xi_j^{(0)}(\nu,\rho)\right\}$$

$$- \Delta T A_{ij}(\nu,\rho)\, C_j(\nu,\rho)$$

for $\nu + \rho = n - 1$ starting with $\nu = n - 1$, $\rho = 0$.

(iii) Compare $\xi_2^{(0)}(0,n)$ with the given value. If they agree we accept $\alpha^{(0)}(n,0)$ as correct and proceed to obtain m, c, λ, α for $\nu + \rho = n$ via the Rankine-Hugoniot equations and the difference equations. If they do not agree we make a new guess for $\alpha(n,0)$ and repeat the cycle.

In practice, the trial values of α are not chosen arbitrarily. We take $\alpha^{(0)}(n,0) = \alpha(n-1,0)$, $\alpha^{(1)}(n,0) = \alpha(n-1,0) + \Delta s \dfrac{\partial\alpha(n-1,0)}{\partial s}$, and thereafter determine $\alpha^{(k)}(n,0)$ by "false position."

There exist checked routines for step (i) above, i.e., the solution of the Rankine-Hugoniot equations for ξ_1 and ξ_2, and for obtaining m and c from these equations. These present no particular scaling difficulties. A routine for step (ii) is being written. Here the scaling difficulties are formidable since $A_{ij} = O\left(\dfrac{1}{\lambda(1 - m^2 \cos^2 \mu)}\right)$ and hence, for the initial experiments, the floating point routine A-1 is being used with the restriction $\lambda(1 - m^2 \cos^2 \mu) \geq 2^{-30}$. This will place drastic restrictions on the computation time and available high-speed store, but seems to be desirable in the absence of any real information regarding the range of the dependent variables. In order to handle points $\nu + \rho \leq n$ without reference to the drum it will be necessary to have available approximately 8n locations over those required for the routine and the floating point auxiliary. The necessary routines to finish step (iii) will be written next; these do not seem to involve any new difficulties.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During October specifications were presented for 15 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 876. Numbers followed by T are for theses.

875 Electrical Engineering. Sine and Cosine Integrals. A sub-routine for computing sine and cosine integrals has been prepared which computes integrals using rational fraction approximations.

876 Physics. Diffusion in the Vicinity of an Interface between Alloys of Different Compositions. The second order partial differential equation is solved using standard techniques.

877 Structural Research. Natural Frequencies of a Multi-Story Building Frame with Flexible Girders. Standard library routines are used to find the natural frequencies and mode shapes.

878 Aeronautical Engineering. Solution of a Spherically Symmetric Flow Behind a Shock Wave Generated by a Time Dependent Energy Release. Equations representing the conditions behind the shock are integrated for various representations of the energy release as a function of time. The Runge-Kutta method is used.

879 Computer. NOT Circuit Analysis. This code computes the dc output levels, maximum collector voltage, maximum collector dissipation, and maximum emitter current for a standard grounded-emitter, direct-coupled transistor NOT circuit with specified tolerances on transistor parameters, resistors, and power supply voltages.

880 T Chemistry. Crystal Field Extension. This problem is similar in detail to No. 763.

881 Physics. Neutrino Recoil of A^{35}. Time-of-flight measurement of the atomic reaction of $A^{35} \xrightarrow{B,+2} Cl^{35-}$ are made with the help of a spectrometer. The measurements are to be tabulated using the computer.

882 Electrical Engineering. Antenna Phase Pattern Tables. Tables of $\frac{R}{\lambda}(1 - \cos\alpha)\cos\theta$ for 16 values of λ, each value containing 60 values of α, and 12 values of θ for each α are to be compiled.

883 Computer. Matrix Inversion Routine. The purpose of this routine is to provide machine users with a temporary matrix inversion process which will be improved later.

884 Chemistry. A Statistical Mechanical Treatment of Reaction Kinetics. Three and four-bodied collisions which lead to chemical reactions are examined by solving the Hamiltonian equations obtained by expressing the kinetic energy of these systems in terms of classical mechanics and the potential energy in terms of quantum mechanics. Monte-Carlo procedures will be used to simulate a chemical reaction.

885 Animal Science. Swine Nutrition. A statistical analysis is being made of data from a swine nutrition experiment.

886 Electrical Engineering. Learning Use of the Computer. This problem was to acquaint Mr. Kenyon with the use of the computer.

887 Physical Chemistry. Radio Frequency Distribution. Radio frequency spectra have been obtained for various samples. These spectra are to be used for computing inter-atomic distances and information concerning the motion of groups of atoms in a molecule, and the potential energy barriers associated with the motion of these groups. The second moment of the frequency distribution curve is used to calculate the inter-atomic distances. The frequency distribution curve itself is obtained by integrating the observed data.

888 Physics. Momentum Correlation for Proton-Proton Collision. Proton-proton collisions have been observed in photographic emulstions exposed to 6.2 bev protons. By knowing the total energy and momentum of the system, one may calculate a possible range of values for the momentum of one particle using the momentum of the other particle as a parameter.

889 Electrical Engineering. Zetetics. A routine has been written to calculate the set sum and set product of a number of sets whose elements are given.

Table I shows distribution of machine time for the month of October.

TABLE I

Regular Maintenance	46:25
Unscheduled Maintenance	24:01
Drum Engineering	27:11
R.A.R.	5:28
Leapfrog	85:47
Wasted	:00
<u>Use by Departments</u>	
Computer Group	11:53
Physics	14:50
Control Systems Lab.	45:25
Structural Research	6:25
Struct. Res. (AF 24994)	2:02
Struct. Res. (DA-11-02-ORD1980)	:25
Struct. Res. (AF 170 T-POT)	:14
Electrical Engineering	1:42
Elec. Eng. (AF 3220)	1:41
Elec. Eng. (NOBSR 64723)	:10
Psychology	24:02
Psychology (MD 620)	10:31
Psychology (MD 569)	4:08
Chemistry	49:17
Agriculture	19:01
MURA	155:16
Ill. Dept. of Public Welfare (Coan)	14:59
Ill. Dept. of Public Welfare (Hurley)	:45
Classes	4:27
Demonstrations	3:26
Miscellaneous	12:06
	571:37

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for October.

TABLE III

Reader Errors	2
Punch Errors	2
Control Errors	4
Memory Errors	1
Drum Errors	5
Arithmetic Unit Errors	2
Power Failure	1
Total Errors	17

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
10/1/56	20:00	:00	0		00	2:05	0
10/2/56	18:40	1:20	1	(1) Leapfrog error probably due to a tube or sockets in RII or RIII.	00	2:34	1
10/3/56	20:00	:00	0		00	1:51	0
10/4/56	19:59	:01	1	(1) Sum check error in reading leapfrog from drum	00	2:05	1
10/5/56	19:55	:05	1	(1) Light burned out on reader B	00	1:22	0
10/8/56	20:00	:00	0		00	:49	0
10/9/56	19:59	:01	1	(1) Drum went out of "synch". Noticed lights dimmed, probably momentary voltage drop.	00	:43	0
10/10/56	20:00	:00	0		00	1:30	0
10/11/56	19:59	:01	1	(1) Control error possibly in division hang-up circuit.	00	2:38	0
10/12/56	19:05	:55	1	(1) Memory, action sense pulser was not operating properly	00	1:27	0
10/15/56	15:16	4:44	1	(1) Tube 51-(6AL5) in arithmetic control shorted. Leapfrog first failed and then, computer failed to operate at all	00	1:04	1
10/16/56	19:59	:01	1	(1) Drum Failure	00	3:43	0
10/17/56	20:00	:00	0		00	1:52	0
10/18/56	15:03	4:57	2 See Note Below	(1) Replaced tape reader control chassis, morning Eng. ran over until 4:45 PM (2) Shorted tube 30 in new control chassis	00	1:04	0
10/19/56	19:03	:57	2	(1) Punch No. 5 failed to punch 2 hole (2) Reader B error	00	2:13	0
10/22/56	20:00	:00	0		00	1:02	0
10/23/56	15:26	4:34	2	(1) Punch No. 5 failed to punch a 4 hole	00	:49	0

TABLE II

Date	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
				(2) L4 failures. Tube 67 in memory control failed to turn over. Adjusted power supply so computer could run temporarily and then tubes were checked.			
10/24/56	20:00	:00	0		00	1:23	0
10/25/56	19:59	:01	1	(1) Drum Failure	00	:53	0
10/26/56	20:00	:00	0		00	:56	0
10/29/56	20:00	:00	0		00	7:53	0
10/30/56	19:51	:09	1	(1) AC power breaker for -300V power supply opened for unknown reasons.	00	9:22	1
10/31/56	19:59	:01	1	(1) Drum Failure. Track 16 N.	00	11:48	0
				The installation of a new tape reader control chassis on October 18 required more time than anticipated. This new chassis adds a "sprocket hole time" to the time allowed for braking before an error would occur. Fifteen interruptions or errors occured during the period through October 23, directly as a result of this new chassis. These fifteen interruptions or errors are not listed in the above table although the time to find the trouble or repair is included in the repair time of the table.			
TOTALS	442:13	17:47	17		00	61:06	4

Reports and Seminars

Seminars

"A Proposed Order Code for a High-speed Computer," by J. H. Fishel, October 2, 1956.

"An Industrial Computer Organization," by C. C. Farrington and G. H. Golub, October 9, 1956.

"Millimicrosecond Pulse Techniques," by Gene H. Leichner, October 16, 1956.

"On the Derivation of Difference Equations for Hydrodynamics," by Prof. A. H. Taub, October 23, 1956.

"Fast Magnetic Memories," by Prof. R. W. McKay (University of Toronto and University of Illinois), October 30, 1956.

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UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

November 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

Design of Arithmetic Unit

The following topics outlined in the October report were considered and worked out in detail during the month of November:

1) A carry-completion circuit to be used in conjunction with the carry assimilation circuitry of the proposed adder has been designed.

2) The sensing circuitry for multiplication by sensing two digits at a time was considered and the requirements were set up in tabular form. Included were all special cases:

If, as proposed, a multiplication of a negative multiplier y by a multiplicand x is performed as (-x)(-y), yielding a positive machine multiplier, a negative multiplier correction is not necessary, unless y = -1. Whenever the signs of multiplier and multiplicand differ, though, a negative multiplicand correction is necessary. A method for the latter correction is known, but investigation of other methods is warranted.

The case of a multiplier of (-1) has been included in the consideration. An extra step is also required if the absolute value of the multiplier exceeds 2/3.

Several other problems arose in the process of designing the multiplication sensing circuitry, such as the necessity of a partial carry assimilation for the digits of the product to be shifted into Q. The cases of either a word having an even number of non-sign digits or an odd number of non-sign digits were considered and led to special steps at the end of each multiplication. The complexity of the control circuitry seems to be about the same in both cases, although an odd number of non-sign digits requires a shift of one position to the right, or a right shift of two followed by a left shift of one. (The left

shift of one is necessary for division; an odd number of shifts in general will require similar arrangement, unless gates are provided for a right shift of one digital position.)

3) One method of division yielding a rounded quotient and correct remainder has been devised, but sensing circuitry has not been worked out in detail.

For reasons of time savings, non-restoring division has been considered. In this case, problems arise from the necessity of converting the quotient. Also, a properly rounded quotient can be obtained only by use of the adder. These considerations seem to indicate that the quotient should end up in $\overline{A}\ \overline{C}$. This topic is still open.

No cost or time estimates have been made so far.

High-Speed Circuits

Design work has been carried out on a number of fundamental computer circuits using diffused base transistors. Recently 30 Western Electric GA-53233 diffused base transistors have been received and experiments are now underway to use them in the circuits which were already designed. Preliminary results indicate that if transistors are selected to have a dc α greater than 0.9, it is possible to have circuits with reasonable tolerances with operation times of about 25 millimicroseconds using these transistors. 13 of the 30 transistors received are acceptable from this standpoint. Although the other transistors can be used as well in some cases, the lower dc α makes their use more difficult from a tolerance standpoint. A report describing these circuits in detail is being prepared.

High-Speed Memories

Equipment is being constructed to study experimentally the problems of current regulation, power dissipation, etc. in the word arrangement memory mentioned in the September report.

Effort in design has also been concentrated on the word arrangement memory. The use of the best techniques with a word arrangement memory may permit an access time of about 1.6 microseconds. Two variations labeled

Memory Design 1 and Memory Design 2 are being studied. The first is essentially the one described in the September report. The second includes several novel features as indicated in the following description.

Memory Design 2: Three features distinguish this design from the first.

(a) Two cores are used to represent each bit and these cores are always in opposite states. As a result a constant load is presented to the pulse generators no matter what word is stored.

(b) A number of cores, identical with the bit cores and forming part of the same assembly planes, are used as switch cores. Heating of the switch cores is thus reduced to the somewhat less serious problem of heating of bit cores, since identical cores are used for both purposes and both switch and bit cores turn over in the same time. Several other advantages also exist which can be demonstrated in a fuller discussion.

(c) Since signals due to reversible flux changes will be more or less equal in the two cores representing any bit they will cancel out in the sensing wires. Any net signal sensed must be produced by irreversible flux changes. In the reading process there is no need to continue reversing the cores after a definite signal has been received. Thus the time required need only be a fraction of the time for complete switching and return of the cores.

Switching Properties of Cores: Experiments on the switching properties of cores have been discontinued. Useful data have been obtained on the reversible flux changes. The irreversible flux changes were not found to be expressible in any reasonably simple form so that it did not seem useful to proceed further.

Boolean Circuit Theory

The first of a series of reports on the theory of asynchronous circuits was completed in November. Work is continuing on a second report which will include material up through the proof that the lattice of C-states is semi-modular. An earlier proof was given in Report No. 66 (December 6, 1955), but the present proofs refer to the new theory on allowed sequences and include the non-binary case. Most of this development is new. Work has also been started on the cycling theory in order to bring it up to date in the same way, and the theory of distributive circuits is being similarly attacked.

Sorting

For tape merging, a method was devised for block reading and block writing on tapes requiring 2/3 of the usual number of storage locations. For k input tapes and k output tapes, and blocks of size B this requires (2k + 2)B memory locations.

The rules are these:

1) 2 B locations are assigned to each input tape and 2 B locations to merge into for output B-size blocks.

2) Read in one block from each tape, and estimate, by comparing the last element of each block, which region will need refreshing first.

3) At each stage B words are read in, and B words are output to some output tape, and step 2 is repeated. The only complicated situation occurs when one region contains more than B items, and the test shows that nevertheless it needs refreshing first. Since the total number of items is always kB, there always exists an empty block into which we may read from tape. A small index is required showing the significance of the various blocks.

The importance of this method is that for given core store size larger blocks may be read from tape, thus reducing start-stop time when changing from tape to tape. Alternately more program may be held in the core store for fixed block size.

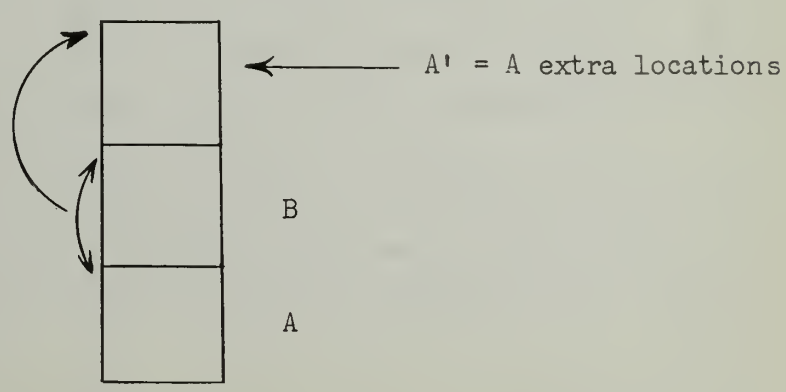
A method for merging has been found which requires only 3N/2 storage location to sort N words. The principle used is this: to merge a block of size A and a block of size B, when

1) $A \leqslant B$

2) The 2 blocks are situated in consecutive locations

3) The additional memory locations follow consecutively after block B (or precede A if we use locations cyclically),

then only A extra locations are required if we merge backwards:



The leading elements of A and B are compared, and the winner occupies the top location of A', and then the next element of the winners' list is compared with the first element of the losers' list, and the resulting winner is sent to the second location of A'.

The resulting merged list occupies A', B. This method has two additional notable features:

1) Variants of it exist requiring max $(2^{n-1}, k)$ extra locations to sort $2^n + k$ words $(0 \leq k < 2^n)$. The rules for these are somewhat complicated, and it would only be worthwhile for large sorts.

2) In the event that some or all of the items in B follow the last item of A, it is not necessary to move them physically in the memory. They remain in their initial locations, so the merge can be discontinued when the last element of A has been inserted.

Register Arrangement

The investigation of an order code for PAC (see previous reports) has shown that the utilization of additional S registers in the arithmetic unit contributes significantly to a reduction in the number of operand accesses involved in many routines. Very little has been gained, however, in the way of a reduction in the number of instruction accesses. In concentrating on solutions to this latter problem a device known as a control memory has been introduced. The study concerning a control memory has not progressed to the stage where any definite remarks can be made as to its effectiveness in reducing instruction accesses. In fact, a suitable design for a control memory is still undecided. However, a general outline of the course this investigation has taken, together with several comments on its applicability, can be made, keeping in mind their conjectural nature.

A control memory may be described as a set of n words, each containing a sequence of orders. The orders may be macro-orders which perform a complete operation, such as Illiac orders, e.g., multiply α by β, or divide α by β; or the orders may be micro-orders which perform fundamental machine operations, e.g., gate from A' to A, or transfer the contents of S_1 to R'. The construction of a word in the control memory determines how many orders it contains.

Under certain conditions, viz., when a series of arithmetical operations to be carried out requires no reference to the high speed memory, one word from the control memory could conceivably carry out a number of operations which might

require several words of the high speed memory. This would eliminate much wasted time due to instruction accesses. Thus when such a condition arises in a routine the control would be instructed to discontinue its normal operation of executing orders received from the high speed memory and execute the sequence of orders contained in a specified word in the control memory.

A control memory [C], for our purposes, will be a set of 16 words. Each word is made up of 40 binary digits and can be packed with 4 abbreviated orders. An abbreviated order is one which allows 8 binary digits for the instruction and 2 binary digits for the address. Thus the makeup of an instruction in an abbreviated order is entirely analogous to the Illiac instruction; the address, however, is restricted to 4 locations.

Associated with [C] is an order register $\bar{R}_3$ and a companion register $\bar{\bar{R}}_3$, with gates for transferring digits from $\bar{\bar{R}}_3$ to $\bar{R}_3$. The function of $\bar{R}_3$ is similar to that of the Illiac order register R_3. That is, when a word from [C] is transferred to $\bar{R}_3$, the left hand order is executed first. The instruction digits are sent to the decoding register and the address digits are sent to either the address generator or the shift counter. After this order has been completed the next order is executed and so on until all 4 orders have been completed. At this time a second word from [C] which was transferred to $\bar{\bar{R}}_3$ at the same time the first word was transferred to $\bar{R}_3$ is gated to $\bar{R}_3$ and the next 4 orders are executed. Also associated with [C] is a number register $\bar{R}^3$ which receives an operand from the high speed memory while the words from [C] are being transferred to $\bar{R}_3$ and $\bar{\bar{R}}_3$. Thus the instruction access time involved in [C] is absorbed by the operand access time required by $\bar{R}^3$.

The orders referring to C are:

YN (n) and

ZN (n)

Y specifies that [C] is to be used and instructs the control to transfer words N and N + 1 from [C] to $\bar{R}_3$ and $\bar{\bar{R}}_3$ respectively. (n) specifies the address of the operand to be transferred to $\bar{R}^3$. After the 4 orders of N are executed $\bar{\bar{R}}_3$ is gated to $\bar{R}_3$ and the 4 orders of N + 1 are executed. When Y is replaced by Z, $\bar{\bar{R}}_3$ is immediately gated to $\bar{R}_3$ so that just the 4 orders of N + 1 are executed.

YN (n) may be either a right hand or a left hand order of a word in the high speed memory. When this word is transferred to R_3, if YN (n) is a left hand order the control executes this order and then executes the orders in $\bar{R}_3$ and $\bar{\bar{R}}_3$ before executing the right hand order in R_3. If YN (n) is a right hand order the

control executes it and then executes the orders in $\bar{R}_3$ and $\bar{\bar{R}}_3$ after which the next order pair is transferred to R_3 from the high speed memory.

The orders forming a word in [C] are of the standard Illiac (PAC) type: TV (n), but T is restricted to be 0, 1, 4, 5, 6 or 7 (plus similar PAC orders, eg., M, N, A, etc.). If the instruction TV requires an address, then (n) refers to S_1, S_2, S_3 or $\bar{R}^3$, while if TV indicates a shift then (n) indicates the number of shifts (which must be less than 4).

An example follows for illustrative purposes. This example uses a repeat order: RR(n). When RR(n) is a left hand order the right hand order of that word is repeated n times, the address being increased by 1 each time the order is repeated.

<u>Exponential (S2):</u> This routine would be written as follows when programmed for PAC-3. It is assumed that the repeat order is available and that the argument -x is in S_1 when the routine is entered.

0	K5	F	5	LS_1	m	9	LS_1	S_2
	42	10L		41	F		SS_2	F
1	50	S_1	6	RR	4	10	NJ	S_2
	01	3F		NS_1	m+1		22	[F]
2	L4	3L	7	$7S_3$	S_2		.	Constants
	42	8L		50	S_3		.	
3	11	3F	8	7J	S_1		.	
	S5	11L		50	[F]		.	
4	LS_2	n						
	51	S_2						

W: 11 prog.
14 const.

OA: 10

IA: 11

TS: 0

The same routine programmed for PAC-3, using [C], would be as follows:

0	K5	F	3	Z1	n	6	waste	
	42	6L		LS_1	m		22	[F]
1	50	S_1	4	RR	4		.	Constants
	01	3F		NS_1	m+1		.	
2	F4	L	5	waste			.	
	42	5L		Y0	[F]		.	

$[C]$

0	$7S_3$	S_2
	50	S_3
	7J	S_1
	LS_1	S_2
1	50	$\bar{R}^3$
	SS_2	F
	NJ	S_2
	waste	
2	11	3F
	S5	F
	LS_1	$\bar{R}^3$
	51	S_2

W: 7 prog. / 14 const. } high speed mem; 3: C

OA: 10

IA: 7

TS: 0

As inefficient as this program appears to be (due to the waste orders) there is still a reduction of 4 instruction accesses out of the original 11.

$[C]$ is not as easily adapted to all routines, however. The IA in the Square Root Routine is not reduced to any extent but this is due to the nature of the calculation. In other routines, e. g., the Logarithm Routine S3, the absence of any reduction in IA when using $[C]$ suggests the need for additional features in the design of $[C]$. For example, when transferring control to the word in $\bar{R}_3$ one might wish to begin with the third order instead of the first; or one might wish to terminate the use of the word in $\bar{R}_3$ after executing the third order. The frequency of occurrence of such problems, however, has not been determined.

The size of $[C]$ may not be adequate for sizeable programs. It is therefore assumed that both complete and partial substitutions may be made in any word in $[C]$. On the other hand, it may be desirable to designate several words of $[C]$ as fixed. For example, if the order

NS_1 (n) : (1) $[Q \cdot S_1 + 2^{-39} A] + n = A'Q'$

(2) $A' \longrightarrow (S_1)$

(3) $Q' \longrightarrow (A)$

(4) reset Q

is in great demand but is impractical as a single order, it could be carried out by:

p	ZN (n) reset Q

$$N + 1 \left\{ \begin{array}{ll} 75 & S_1 \\ L4 & \bar{R}^3 \\ 40 & S_1 \\ S5 & F \end{array} \right.$$

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Floating Address Routine and Drum Storage of Library Routines

The floating address routine is now stored on the magnetic drum and the character K will call the program into use. Two changes were made to increase the speed of the program: (1) storage of blocks of programs on the magnetic drum and (2) shifting instead of multiplying by ten. An ordinary program using the Decimal Order Input will require about one third more input time when using the floating address routine than it would using the Decimal Order Input alone.

Library routines will be recorded on the magnetic drum using routine Y-3 and will be played back by use of a modified version of Y-2. When a directive of the form (R1) OOnK is read from the input tape, a search is made to see if routine R1 is stored on the magnetic drum. If it is, it will be played back into a set of Williams memory locations beginning with location n. If R1 is not stored on the magnetic drum a stop with an appropriate signal occurs.

Program Library

During November the following program was added to the auxiliary library.

Q-4 (228) Single Circuit Analyzer. Complete Program. This program is a modification of library routine Q-3 and is used whenever a circuit exceeds capacity of Q-3. It provides in excess of a fifty percent increase in the number of states per cycle.

PART III

MATHEMATICAL ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794.)

Several programs have been written for studying the propagation of discontinuities for various difference replacements of the equation

$$u \frac{\partial \rho}{\partial x} + \frac{\partial \rho}{\partial t} = 0 \qquad (1)$$

with u constant as a function of $\frac{u \Delta t}{\Delta x}$, for two types of initial and boundary conditions:

(1) ρ given for all x at t = 0

(2) ρ given for $x \geq 0$ at t = 0
and at x = 0 for $t > 0$.

The purpose of this study is to determine rules for selecting difference replacements for the equations of hydrodynamics (eq. (1) being a special case of one of these) for various given initial and boundary conditions.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During November specifications were presented for 14 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 890. Numbers followed by T are for theses.

890 T Food Technology. Packaging of Orange Juice. The program will analyze variances and covariances on subjective and objective data collected in the study of packaging orange juice in plastic bags.

891 Electrical Engineering. Aperture Admittance. The program will compute aperture admittance of a rectangular wave guide with varying aspect ratio.

892 Psychology. Personality factors in Four and Five-Year Old Children. Statistical analyses are made of personality factors in four and five-year old children. These factors include parent and teacher ratings and time sampling records.

893 University of Rochester, Department of Psychology. Mood Study. Moods were induced in groups of 500 college men by use of movies and in one case by use of a hoax. The subjects were then given a test involving the use of words. Statistical studies of the correlations between moods and test results will be made.

894 University of Michigan, Department of Psychology. Twin Study. The computer is used to analyze the correlations between several selected characteristics of 82 pairs of twins, some of whom are fraternal and some of whom are identical.

895 T Mathematics. Monte Carlo Investigation of Some Learning Models. Several mathematical models have been prepared which offer a description of the learning processes. Some of these models whose predictions cannot be made with sufficient specificity by analytical means are to be investigated by Monte Carlo methods.

896 Computer. Reader Timing. This program is to be used to obtain the variation of reader speed with the time spent within the reading loop. The information obtained by use of this routine will aid in preparation of input sub-routines for the Illiac Library.

897 Structural Research. Stiffness of Carry-Over Factors for Orthotropic Plates. This investigation is concerned with the analysis of orthotropic plates simply supported along two opposite edges and continuous in other directions over a series of rigid or flexible supports transverse to the simply supported edges. The present program evaluates expressions for stiffness, carry-over factors and the product of these quantities, for values of the relative stiffness parameter less than one.

898 Student Counseling Bureau. Structural Analysis of Ewing Personal Rating Form for Self-Description. Structural analyses are being made of results obtained from the Ewing Personal Rating Form. These analyses are to be used to study the internal structure of the form.

899 Mechanical Engineering. Heat Distribution in Metal Cutting Tool. Several parameters are varied in order to obtain various distributions of heat. These distributions are tabulated.

900 T Theoretical and Applied Mechanics. Fatigue Damage During Complex Stress Histories. Experimental results obtained by subjecting a specimen to cyclic stress of varying amplitudes are set into a formula giving the theoretical number of cycles to failure. Parameters are adjusted to give the best fit.

901 College of Medicine. Method for By-passing Factor Analysis. A new method of by-passing factor analysis is being developed. This involves selecting groups

of people who are relatively alike on groups of measures; the efficiency of this method is being tested experimentally by use of statistical data.

902 University of Michigan, Department of Electrical Engineering. Radiation Pattern. This program is designed to compute the radiation pattern of an array of magnetic dipoles on the surface of a conducting sphere.

903 Institute of Communications Research. Content Analysis. Approximately 60 content analysis variables will be used to analyze 70 messages. The 70 messages were selected to provide a broad sample of material. A factor analysis is to be made of these variables.

Table I shows distribution of machine time for the month of November.

TABLE I

Regular Maintenance	49:13
Unscheduled Maintenance	7:27
Drum Engineering	26:09
R.A.R.	5:21
Leapfrog	50:20
Wasted	:00
<u>Use by Departments</u>	
Computer	13:30
Physics	24:40
Control Systems Lab.	38:19
Structural Research	10:35
Struct. Res. (AF 24994)	16:00
Psychology	29:06
Psychology (MD 620)	9:51
Psychology (MD 569)	1:06
Public Health Dept. (3M9067C)	:18
Electrical Engineering	1:55
Elec. Eng. (AF 3220)	:39
Elec. Eng. (Nobsr 63723)	:29
Chemistry	37:09
Agriculture	16:27
College of Medicine	:46
Mech. Eng. (ORD 1980)	:10
MURA	99:43
Univ. of Mich. (Psychology Dept.)	1:05
Univ. of Mich. (Elec. Eng. Dept.)	:07
Univ. of Rochester (Psychology Dept.)	11:34
Classes	20:38
Demonstrations	2:05
Miscellaneous	29:23
	504:05

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for November.

TABLE III

Reader Errors	3
Punch Errors	4
Drum Errors	10
Memory Errors	1
Control Errors	2
Arithmetic Unit Errors	1
Scope Errors	2
Total Errors	23

TABLE II

Date	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
11/1/56	19:58	:02	1	(1) Punch #5 error. Failed to punch 4 hole.	00	1:56	0
11/2/56	19:48	:12	2	(1) Reader "B" light went out.	00	2:15	0
				(2) Reader "B" light had foreign particle in it which was throwing a shadow on tape causing reader errors.			
11/5/56	20:00	:00	0		00	1:13	0
11/6/56	19:59	:01	1	(1) Drum out of synch.	00	:50	0
11/7/56	19:59	:01	1	(1) Drum out of synch.	00	4:01	0
11/8/56	19:59	:01	1	(1) Drum error.	00	1:13	0
11/9/56	19:59	:01	1	(1) Lost synch.	00	1:13	0
11/12/56	20:00	:00	0		00	1:26	0
11/13/56	20:00	:00	0		00	2:55	0
11/14/56	19:58	:02	2	(1) Drum error	00	1:45	1
				(2) Leapfrog. Sum check incorrect on first attempt (arithmetic error?).			
11/15/56	19:58	:02	2	(1) Drum error.	00	:50	0
				(2) Scope error.			
11/16/56	20:00	:00	0		00	1:11	0
11/19/56	19:42	:18	1	(1) Reader "B" error.	00	:51	0
11/20/56	19:59	:01	1	(1) Scope error.	00	:53	0
11/21/56	19:58	:02	2	(1) Drum error.	00	1:08	0
				(2) Drum error.			
11/23/56	20:00	:00	0		00	:42	0
11/26/56	19:53	:07	1	(1) Control error.	00	1:54	0
11/27/56	18:31	1:29	2	(1) Memory failure 2^{-7} changed chassis.	00	1:39	0
				(2) Drum error.			

TABLE II

Date	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
11/28/56	19:36	:24	3	(1) Punch #3 error - tape broke. (2) Punch #3 error - brake too tight. (3) Drum error.	00	:59	0
11/29/56	19:58	:02	2	(1) Leapfrog, punch #5 error, failed to punch "8". (2) White switch error.	00	4:25	2
11/30/56	20:00	:00	0		00	2:35	0
Totals	417:15	2:45	23		00	35:54	3

Reports and Seminars

Seminars

"The Sorting Problem," by D. B. Gillies, November 6 and 13, 1956.

"A Proposed Fixed Point Binary Arithmetic Unit," by Prof. J. E. Robertson, November 20, 1956.

"Application of Illiac in Data-Processing in Agricultural Economics," by Profs. V. I. West and E. A. Swanson, Agriculture Economics Dept., November 27, 1956.

Reports

Digital Computer Laboratory Report No. 75, "A Theory of Asynchronous Circuits I," by D. E. Muller and W. S. Bartky.

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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

Part I: Study Program on High Speed Computer

Part II: Mathematical Research and Programming

Part III: Mathematical Analytical Program

Part IV: Illiac Use and Operation - General Laboratory Information

December, 1956

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

Design of Arithmetic Unit

Previous progress reports have discussed an arithmetic unit in which a separate carry register is used. It is important in such a unit to consider the problem of overflow and the extent to which the carries must be assimilated in order to detect overflow.

Conventional Overflow Analysis: If an arithmetic unit without separate carry storage is designed with negative numbers represented as complements with respect to 4 (i.e., with the arithmetic unit extended one digit to the left of the sign digit of a two's complement unit), it is possible to determine overflow if a number x is outside the range $-1 \leq x < 1$, provided the range $-2 \leq x < 2$ is not exceeded. The ranges indicated by the two digits x_{-1} and x_0 to the left of the binary point are then

x_{-1}	x_0	Range of x
0	0	$0 \leq x < 1$
0	1	$1 \leq x < 2$
1	0	$-2 \leq x < -1$
1	1	$-1 \leq x < 0$

If x in the range $-2 \leq x < 2$ is represented as a complement with respect to 2^n, then x_{-1} is representative of all digits of greater significance; i.e. $x_{-i} = x_{-1}$ for $i = 2,3,\ldots,n-1$.

Indicated Ranges for Arithmetic Unit with Separate Carry Storage: In an arithmetic unit with separate carry storage, a number x is represented as a complement with respect to 4 by two sets of digits a_{-1} a_0, a_1, ..., a_{39} and

$c_0, c_1, \ldots, c_{38}$ with the a_i in the accumulator and the c_i in the associated carry register. Employing the relationship $c_{i-1}\, a_i = 0$ for $i = 1, \ldots, 39$ we can deduce from the digits a_{-1}, a_0, c_0, the following information concerning the range of x.

a_{-1}	a_0	c_0	Range of x	
0	0	0	$0 \leq x < 1\ 1/2$	
0	0	1	$1 \leq x < 2$	x lies outside the range $-1 \leq x < 1$
0	1	0	$1 \leq x < 2 \quad -2 \leq x < -1\ 1/2$	
0	1	1	$-2 \leq x < -1$	
1	0	0	$-2 \leq x < -1/2$	
1	0	1	$-1 \leq x < 0$	x is within the range $-1 \leq x < 1$
1	1	0	$-1 \leq x < 1/2$	
1	1	1	$0 \leq x < 1$	

(If x is represented as a complement with respect to 2^n, then $a_{-i} = a_{-1}$ and $c_{-i} = c_{-1} = 0$ for $i = 2,3,\ldots,n-1$.)

In essence, the effect of the carry assimilation is additive and can, if $c_0 = 0$, increase the sum $2a_{-1} + (a_0+c_0)$ by one unit. If $c_0 = 1$, the assimilation of carries will not affect the sum $2a_{-1} + (a_0+c_0)$ and the results of the conventional overflow analysis can be applied with $2x_{-1} + x_0 = 2a_{-1} + (a_0+c_0)$ [modulo 4].

From the table it is apparent that three cases arise:

1) The unassimilated results indicate definitely that x lies outside the range $-1 \leq x < 1$. This unassimilated overflow occurs when a_{-1}, a_0, and c_0 have states 001, 010, or 011.

2) The number x may or may not lie outside the range $-1 \leq x < 1$ after assimilation. (States 000 and 100 of a_{-1}, a_0, and c_0)

3) The number x is definitely in the range $-1 \leq x < 1$. (States 101, 110, 111 of a_{-1}, a_0, and c_0).

It is important to distinguish between unassimilated overflow (Case 1) and assimilated overflow which may occur in Case 2. It has been shown in a

detailed analysis that it is sufficient to detect unassimilated and assimilated overflow separately without the necessity for assimilation for the sole purpose of detecting overflow for several arithmetic operations. These operations which have been considered are:

1) overflow on left shift,
2) overflow during addition or subtraction,
3) arithmetically correct right shift for multiplication.

High-Speed Circuits

Reports are being prepared on one set of basic computer circuits using the Western Electric GA-53233 transistor. A study of saturation in these transistors has shown that if precautions are not taken to keep the transistors from becoming saturated, the delay time in the transistor can amount to 100 mμs or more. Although additional design work is proceeding with these transistors for a half-adder and combinations of the basic circuits including registers and counters, the shortage of the transistors makes it impossible to carry out experimental work on these more complex circuits.

High-Speed Circuits

The last report indicated that design effort was being put into a word arrangement memory which may permit an access time of about 1.6 microseconds. It is intended that this memory would have between 1000 and 4000 words and would be generally considered to be the internal memory for the machine.

In a machine in which the operation of addition might require only about 0.2 μs and the operation of multiplication not more than 5 μs, it seems clear that the over-all balance of the machine could not be considered to be good unless a memory is available with an access time of about 0.1 μs. Although a memory with such a short access time would be very expensive if it had a large number of words, it is possible that the design would be fairly reasonable if the number of words were restricted to less than 100. One approach to this has been that of an electromagnetic delay line memory using the high-speed circuits in a simple serial memory. A very simple test of a memory of this kind storing eight bits in 300 mμs has been run. It is evident that it would

be possible to use a serial memory of this kind for each bit position in a word, thus allowing an average access time of 150 mμs for any one of eight words in a parallel machine. A technical report on this memory is being prepared.

Two other forms of high-speed small capacity memories may be considered. A diode capacitor memory of the kind worked on at the National Bureau of Standards might be reasonable for perhaps sixty-four words with an access time of less than 200 mμs and variations on existing electrostatic memories may be considered. In a conventional Williams memory, the large number of bits per tube and freedom from read around errors require that the spot location be very accurately determined. If the number of spots per tube face could be reduced to about sixty-four, it is possible that the access time could also be reduced. No work has been done here on either of these two types of memories in this speed range.

Boolean Circuit Theory

The first write-up of the theory of cumulative states and the theory of cycling in semi-modular circuits has been completed, and part of the theory of distributive circuits has been written. Most of the new developments have been in connection with cycling theory as applied to non-binary circuits. This has meant an almost completely new treatment of the theory. In the theory of distributive circuits it was shown that the requirement that a lattice of cumulative states be distributive is equivalent to the statement that the greatest lower bound of any two elements be equal to their numerical intersection. A new proof was obtained for the theorem that the join-irreducible elements in a distributive lattice of C-states correspond to the components of these states. A new theorem has been obtained in the theory of ideals and break sets to the effect that there is a one-to-one correspondence between the ideals and the break sets.

The revision of Library Routine Q-3 was checked and handles most circuits properly. There are several details to clean up before the routine can be placed in the library.

Register Arrangement

Investigation of a control memory [c] is being continued. Application of [c] to the Square Root Routine, R-1, has produced the following results in access

times:

	Illiac	PAC-3	PAC-3 with [c]
W	9	8	5 + 2 [c]
OA	4 + 6n	1	1 + n
IA	4 + 5n	3 + 5n	2 + 3n
TS	3	0	0

n = number of iterations.

This indicates little advantage in the use of [c] with PAC-3. Even less of an advantage is shown using the Logarithm Routine, S-3. It is planned to undertake a more extensive application of [c], e.g., to the Numerical Differentiation Routine, E-4, which might suggest constructive modifications in design.

Sorting

Work is continuing on a study of sorting methods to determine optimum logical structure of a computer for various kinds of sorting applications. The Illiac will be used for some experiments which it is expected will lead to techniques for measuring the effect of increased sorting efficiencies upon program complexity and access to auxiliary memories.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Use of the Magnetic Drum Memory

The combined post mortems routine was completed and placed on the drum. This replaces eleven present routines now used under various circumstances by the computer operator, four of these routines being of considerable importance. These four are the address search routine and print-out routines for order pairs, decimal fractions and decimal integers. The other seven are floating decimal numbers and sexadecimal and drum versions of all but the address search routine. One thing the combined post mortems routine does not provide is a comparison post mortem (Library Routine C-1).

The floating address routine has been stored on the drum and has been used by the students of Mathematics 385, the programming class, for their second assigned problem. No error in the floating address program was observed. However, it was apparent that interludes are handled very slowly, and it may be desirable to provide a special entry for interludes.

Decisions are now being made about the list of routines to be stored on the drum. It is expected that this list will be changed from time to time as dictated by needs of the machine users. For example, Library Routine A-6, the floating decimal routine with six auxiliaries, has been placed on the drum for use by the students of Mathematics 385 and will be called back into the Williams memory by any program tape which has the character S at the beginning.

The solution of the determinantal equation $|A - B| = 0$ is now being programmed for the drum.

Program Library

F-5 (229) Integration of a System of Ordinary Differential Equations up to a Specified Value of One Variable. The features of the older routines HF-1 and F-1 are combined in this routine and some additional features have been added to make the routine more convenient to use. Integration of a system of ordinary differential equations

is carried out by the Gill-Kutta method to the point where a selected variable nears a specified value. At this time the step interval is varied in accordance with the Newton-Raphson formula so as to make this variable coincide with the specified value.

V-9 (216) Generate 40-Bit Random Numbers. A new method, described in Report No. 74, is embodied in this program to generate pseudo-random numbers. It involves forming a linear combination of five previously generated numbers, in which one of the numbers in the linear combination has been shifted circularly. Since no multiplication instructions are used, the method is exceptionally fast. The method has passed several tests for randomness and has been shown not to repeat during the first 10 million numbers.

PART III

ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794.)

Various special solutions of the Einstein field equations have been found. These assume that space-time is plane-symmetric and that the gravitational field is generated by a perfect fluid which is not at a constant entropy. Various additional assumptions are made in order to obtain exact solutions of the equations. For example, if it is assumed that the space-time is static in a particularly chosen coordinate system, exact solutions can be found in which the pressure distribution may be arbitrarily prescribed. Another example is furnished by assuming that the pressure of the fluid is everywhere zero. In this case, too, exact solutions of the field equations may be found.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During December specifications were presented for 13 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 904. Numbers followed by T are for theses.

904 Structural Research. Moment Distribution on Frames with Axial Loads. This problem is a continuation of the problem described in Problem Specification 759. In this problem the effect of axial load on stiffness, carry-over, and fixed-end moment is considered.

905 Structural Research. Two-axle Loading on Simple Beams. Dynamic response of a bridge to vehicles is represented by a set of three simultaneous second-order differential equations. Coefficients of these equations are varied but the bridge is restricted to only one mode of vibration with two degrees of freedom.

906 Computer. The equations of conservation of momentum, energy, and mass, and the equations of state for an ideal gas are transformed into certain differential-integral equations in which only time derivatives appear. This transformation was chosen because it was felt that a difference-sum representation of these equations could be formed which would produce a more accurate solution than has been obtained from other methods. The accuracy of the numerical solution will be investigated for various difference-sum replacements of the differential-integral equations in describing shock wave propagation and the mixing of gases.

907 T Physics. Single Pion Production. Various three-body models of high-energy pion nucleon interactions will be set up in the computer. An incident spectrum of pions will be represented using Monte Carlo techniques and the calculated results will be compared with those obtained experimentally in order to test the validity of the models.

908 Psychology. Alignment of Questionnaire Factors for Ages 4 through 20 Years of Age. Factor analyses will be used to study questionnaires for ages 4 through 20.

909 Mechanical Engineering. Channel Mixing (2-dimensional). Partial differential equations representing the mixing of two gas streams will be solved using difference techniques.

910 T Education. A Factor Analysis of the Illinois Test of Language Abilities. The problem to be solved is a factor analysis of a newly standardized pre-school language test. The purpose of the analysis is to get more information about the test before re-standardizing it.

911 T Chemistry. Calculation of Molecular Conformation in Macrocycles. A macrocycle is a collection of n atoms which are chemically bound. Band lengths and band angles are known. Certain unknown angles will be found by solving a set of non-linear algebraic equations.

912 Computer. Three-dimensional Plotter. This program is a subroutine which may be used to display three-dimensional figures on the cathode ray tube output in such a way that they may be viewed using a stereoscopic viewer.

913 Computer. Automatic Solution of Simultaneous Linear Algebraic Equations. This program has been placed in the Illiac library of routines as Routine L-7. This routine solves up to 143 simultaneous linear algebraic equations in 143 unknowns automatically. It is an extension of the older Routine L-2.

914 Computer. The program computes the phase response as a function of frequency of a minimum phase shift network from given amplitude data on a function of frequency. The time response of the network to a square wave of specified fundamental frequency is also evaluated. The phase response is computed by evaluating a series given by Bode. The square wave response is evaluated by Fourier Series.

915 Dairy Science. Effect of Season on the Metabolic Pattern of Bovine Spermatazoa. This program is to be used to fill in certain missing observations in an experiment testing the seasonal variations of the metabolic pattern of bovine spermatazoa.

916 Chemistry. Relaxation of Non-Equilibrium Distributions. Relaxation methods are to be used for investigating the exchange of energy in inelastic collisions of molecules in a gas.

Table I shows distribution of machine time for the month of December.

TABLE I

Regular Maintenance	29:40
Unscheduled Maintenance	4:39
Drum Engineering	25:52
R.A.R.	5:12
Leapfrog	61:00
Wasted	:00
Use by Departments	
Computer	15:45
Physics	30:06
Control Systems Lab.	41:24
Structural Research	9:38
Struct. Res. (AF 24994)	2:03
Chemistry	49:37
Chemistry (Navy Task 6)	:11
Psychology	26:54
Psychology (MD 569)	2:38
Elec. Eng.	:30
Elec. Eng. (Navy Task 2)	:19
Agriculture	17:31
Mech. Eng. (ORD 1980)	:39
Theor. and Appl. Mech. (Navy Task 53)	:27
College of Medicine	1:54
Ill. Dept. of Public Health	:17
MURA	52:41
Univ. of Michigan	1:08
Classes	20:14
Demonstrations	5:49
Miscellaneous	31:53
Total	438:01

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and the number of failures while the machine was listed as running. During the 5:30-6:00 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for December.

TABLE III

Drum Errors	11
Reader Errors	7
Scope Errors	3
Punch Errors	8
Control Errors (white switch)	1
Total	30

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
12/3/56	19:49	:11	2	(1) Drum error during drum test routine. (2) Drum error indicated by sum check.	00	1:25	0
12/4/56	19:38	:22	3	(1) Drum error during drum test routine. (2) Drum error during drum test routine. (3) Punch #3 error during leapfrog.	00	2:07	1
12/5/56	20:00	:00	0		00	1:03	0
12/6/56	19:56	:04	1	(1) Punch #3 tearing tape.	00	1:17	0
12/7/56	19:59	:01	1	(1) Drum error indicated by sum check.	00	:52	0
12/10/56	19:57	:03	2	(1) White switch transferred control to wrong location (occurred 7 times). (2) Drum error indicated by sum check.	00	:26	0
12/11/56	19:59	:01	1	(1) Bootstrap looped probably due to white switch or drum.	00	:48	0
12/12/56	19:59	:01	1	(1) Two different results from same tapes, possibly reader B error.	00	1:01	0
12/13/56	19:55	:05	5	(1) Two different results from same tapes. (2) 5th hole was not punched. (3) 5th hole was not punched. (4) Drum error. (5) Reader B bulb burned out.	00	:56	0
12/14/56	20:00	:00	0		00	:43	0
12/17/56	19:50	:10	3	(1) Drum error during drum test. (2) Drum error during drum test. (3) Reader B error.	00	1:00	0
12/18/56	19:58	:02	3	(1) Drum error during drum test. (2) Drum sum check error. (3) Punch #3 jammed.	00	3:32	0
12/19/56	20:00	:00	0		00	5:34	0
12/20/56	20:00	:00	0		00	1:41	0

TABLE II (Continued)

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
12/21/56	19:44	:16	2	(1) Failure to punch 5th holes. (2) Reader F had broken photo cell.	00	1:19	1
12/26/56	19:49	:11	2	(1) Film not advancing properly. (2) Film not advancing properly.	00	6:24	0
12/27/56	19:58	:02	2	(1) Failure to punch 5th holes. (2) Reader F error.	00	6:26	0
12/28/56	19:41	:19	2	(1) Punch #3 jammed. (2) Drum error during drum test routine.	00	9:35	1
TOTALS	358:12	1:48	30		00	46:09	3

Reports and Seminars

Seminars

"A Proposed Fixed Point Binary Arithmetic Unit," (Part 2), by G. Metze, December 4, 1956.

"On the Numerical Determination of the Flow behind a Shock in Stationary or Pseudo-stationary Flow past a Given Profile, by D. G. Aronson, December 11, 1956.

"The Design of a Control System for a Digital Computer," by Professor M. V. Wilkes, Mathematical Laboratory, Cambridge University, England, December 17, 1956.

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UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

January, 1957

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

Design of Arithmetic Unit

Investigation was centered on finding a "tidy" division scheme, i.e. a method of division which would yield a truncated quotient and a corresponding remainder whose absolute value is less than that of the divisor.

If we ignore the 39th bit of the quotient formed by the method used in Illiac, we note that the desired features are not obtained if the divisor is negative. This is due to zero being interpreted as a positive quantity. A truncated quotient could then be obtained if it were possible to sense an adder output of zero.

A sensing for zero of the adder output becomes, however, especially complicated if a separate carry storage register is used, as proposed in previous reports. A complete carry assimilation would then be necessary for each step in the division to determine whether or not the adder output is zero.

An alternate method is based on the existence of a positive and a negative zero in the one's complement system of representing binary numbers. It is also known that only negative zeros can result from addition, and only positive zeros can result from subtraction.

The following method of "tidy" restoring division was therefore investigated:

Assume the existence of an arithmetic unit with an adder/subtractor, a device which can either add or subtract, as well as a complimenting circuit available between number register and adder/subtractor. Carry/borrow registers are also used.

Depending on the signs of dividend and divisor, the gates in the arithmetic unit are set as follows:

Dividend	Divisor	Adder/Subtractor	Complementing Circuit
+	+	-	+
+	-	+	+
-	+	-	-
-	-	+	-

Each step of the division process then follows essentially the rules of Illiac division, except for the insertion of the "1" in the least significant place of the quotient.

An attempt was made to devise a division method for a two's complement arithmetic unit such that the attractive features of the one's complement division could be retained. However, it was found that for a double length dividend in two's complement form, it would at times be necessary to subtract a unit from the least significant digit of the adder/carry register. No simple way to perform the subtraction has been found.

An item still under investigation is the design of an adder using base 4 arithmetic. Such a design, although more complex per stage than the equivalent base 2 stages, should cut the length of the carry storage registers in half and may also reduce the time required for carry assimilation.

High-Speed Circuits

Digital Computer Laboratory Report No. 77 discusses one set of basic computer circuits using the Western Electric GA-53233 transistors. For various tolerance reasons, signal size is small and it is not possible to cascade several circuits from this set.

A new set of circuits having 4 volt signal swings instead of the 1.8 volt signal swings of Report No. 77 is now being investigated. A revised routine (#719) is being used to help determine the values of circuit components. Larger signal levels can be tolerated by the GA-53233 transistors if a diode is put in series with the emitter to take up most of the emitter-base back voltage. A large number of design parameters was tried and it was found that, with the limitations imposed by the transistor characteristics, a design for a flipflop would lie in the region where power supply tolerances could be a maximum of $\pm 3\%$, resistor tolerances could

be a maximum of $\pm 3\%$, transistor dc α's must lie in the range 0.93 to 1.00, and it is likely that a diode will have to be used on the transistor collector to clamp them out of saturation. A larger signal swing for the circuits will permit the cascading of possibly four circuits.

Routine #819 was used on the solutions realized from Routine #719 to obtain designs with standard resistor values and even power supply voltages. A number of fair flipflop designs have been found, but none which can be used without a diode to keep the transistor out of saturation. An Illiac routine (#928) has been written for the tolerance analysis of an OR circuit.

A half-adder using the Western Electric transistors has been designed and is being investigated. The half-adder appears to have an operation time of about 45 millimicroseconds. A report on the half-adder is being prepared.

High-Speed Memory

Experimental work is being continued on a core memory with an access time of less than 2 microseconds. As reported earlier, this is based upon a "word access" in which the switch cores are kept separated from the storage cores.

Boolean Circuit Theory

1) Three sections of the second report on speed-independent circuits have been written in their final form and checked. They are concerned with length vectors of $\mathcal{R}$-sequences, development of the theory of C-states, and the theory of cycling.

2) The section on break sets and ideals is now being written. Several new results have been obtained concerning ideals.

a) A set of ideals $H[u, i_1, i_2, \ldots, i_m]$ is shown to describe the apparent behavior of the circuit to an observer who sees only the nodes $i_1, i_2, \ldots, i_m$ in the circuit. The set H is shown to form a lattice.

b) A second set of ideals $K[u]$ is shown to be isomorphic with the set of equivalence sets and to form a sub-lattice of the lattice of ideals. This set is used in predicting the behavior of a circuit in which certain elements fail to act, and to set down rules for determining whether the circuit will stop.

3) The theory of distributive circuits has been written in a rough draft form. A definition of causation was introduced and was shown to be equivalent to the partial ordering of the join-irreducible elements of the lattice of C-states. These elements have the property that they cannot be reduced to a join of two other elements in the lattice; furthermore, they completely characterize the lattice of C-states. A general lattice-theoretic result was obtained which will simplify later theorems concerning the design of distributive circuits. This theorem states that a given join-irreducible element covers a single unique element in the lattice of C-states. This element has the representation as the join of all join-irreducible elements which are covered by the given join-irreducible element in the partially ordered set of these elements. An immediate consequence is that the signal corresponding to such a join-irreducible element cannot occur until all signals which cause it have occurred. This then gives a condition of excitation and hence is applicable to the design theory which will appear in the third report on asynchronous circuits.

4) The extension of Library Routine Q-3 to make use of the magnetic drum was essentially finished, including the description and block diagrams.

PART II

MATHEMATICAL RESEARCH AND PROGRAMMING

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Floating Address Routine

The immediate goal of making a working revision of the floating address routine has now been reached. The revision has been checked out and is now loaded on the drum memory. Like its predecessor it is called for by an initial K.

The following changes have been incorporated:

1) General speeding up of the routine by a number of changes.

2) Introduction of "special interludes" which make use of 26 1102N orders on the tape.

3) The use of 00 K to reset the relativizer.

4) Incorporation of a modified Y-2 routine which will be used to read back library routines placed on the drum with auxiliary Y-3. These routines will be called for by orders ( ) 00 n K or ( ) 00 K where the outside address contains the library designation of the routine. For example (A3) 00 500 K asks that A3 be placed in the program with first word at 500.

5) Special handling for words stored at locations 3 to 15 so that S-parameters may have right-hand inside addresses when read into the computer from the tape reader.

6) Diagnostic Error Control. Types of errors handled are:

a) Same outside address placed before words being stored at <u>different</u> parts of the program. The computer prints a list of floating addresses, addresses of two words in program having this outside address and the floating address in question.

b) Inside addresses not matched by an outside address. The computer prints a list of floating addresses, address of word having inside address and the floating address in question.

c) S-parameters having right hand inside addresses which have not been matched by an outside address when the parameter is called for. The computer prints ST or SD depending on whether source of word using S-parameter is the tape reader or the

drum memory and same information as for (b).

d) Calling for a subroutine not placed on the drum. Computer stops on an FF order.

When errors a, b, c occur, the computer continues assembling the program until the first interlude which requires substitution of true addresses into the program. Special interludes and interludes resulting during playback of library subroutines from the drum memory do not require such substitutions and the computer will not stop. The computer makes all possible substitutions, setting to zero the addresses of words where there are errors. The program is then placed in the Williams memory and an FF stop at 1014 is made.

7) Changes were made so that a word may have any number (not exceeding machine capacity) of outside addresses.

8) Changes were made so that whenever an inside address has already been matched by an outside address the "true value" is substituted while the word is being read in. One consequence of this is that the programmer may start an interlude at location (A) by the order pair 26 (A) 26 1N on his tape. Unlike the D.O.I., the floating address routine always transfers control to the right side of location 1 when beginning an interlude.

Matrix Operations

The new version of Library Routine M-5, which solves the determinantal equation $|A - \lambda B| = 0$, has been checked and is being written up. It is more accurate than the previous version.

Program Library

L-7 (230) Automatic Linear Equation Solver with Programmed Checks and Calculation of Residues. This is an automatic routine using L-6. It is arranged so that the coefficients of a set of up to 143 simultaneous linear algebraic equations may be typed on tape and read into the computer and the roots printed. Various checks are incorporated in the program, and residues may be formed by use of an auxiliary program.

PART III

ANALYTICAL PROGRAM

(This work is supported in part by National Science Foundation Grant G-2794.)

A paper on the conditions that must obtain across singular hypersurfaces in space-time has been prepared and submitted to a technical journal. A variational principle from which the field equations of general relativity and the equations of motion of a perfect fluid may be derived is generalized to allow for the presence of hypersurfaces on which the fluid variables and the metric tensor may be singular. The field equations, the equations of motion and the conditions which must hold across these singular hypersurfaces are determined. The results obtained are shown to reduce to those previously given by O'Brien and Synge. A transformation of coordinates with a discontinuity in second derivatives across the hypersurface is shown to reduce the requirements on the $g_{\mu\nu}$ to be that it and its first derivatives must be continuous across the hypersurface in the new coordinate system. The results are shown to include the generalization of the Rankine-Hugoniot equations for hydrodynamical shocks and to apply to other problems for which variational principles exist.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During January specifications were presented for 13 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 917. Numbers followed by T are for theses.

917 Physics. Kinetic Theory of Shock Waves. The molecular velocity distribution in a strong plane shock wave in a gas is to be found by finding the steady state solution of Boltzmann's differential equation. The collision integral is to be evaluated numerically by a stochastic method.

918 Electrical Engineering. Array Patterns. Given the element pattern of one antenna and the desired feed, the problem is to compute the array pattern over a frequency band for several elevation angles. Solution is by summing complex products and displaying modulus of the result on the oscilloscope.

919 Animal Science. Analysis of Swine Nutrition Data. This is a swine nutrition experiment, studying the effect of free-choice rations and complete rations, both on pasture and dry-lot as measured by weight gains. Four different breeds of swine were used in order to determine whether different breeds of swine react differently to these various treatments. Statistical analyses will be made of the effects of these treatments.

920 Electrical Engineering. Parabolic Reflector. The problem consists of computing the electric field within a truncated parabolic reflector produced by a series of sources near the focus.

921 Mechanical Engineering. Exhaust Process Analysis in an Internal Combustion Engine. In an internal combustion engine, it is desired to compute the crank angle, cylinder volume, cylinder pressure, valve area and the weight of gas remaining in the cylinder during that part of the exhuast blowdown when the Mach number past the valve is 1.

922 Structural Research. Stresses in a Fracturing Plate. Static stress distribution in steel plates during fracture is to be calculated in order to develop hypotheses concerning brittle fracture propagation.

923 Structural Research. Fixed-end Moments and Shears in Orthotropic Plates Due to a Line Load for $\rho > 1.0$. This program evaluates the expressions for fixed-end moments and fixed-end shears in orthotropic plates simply supported along two opposite edges, and subjected to a sinusoidally varying line load in a direction perpendicular to the simply supported edges.

924 T Animal Science. Ovulation in Crossbred Swine. Information concerning ovulation data in gilts over a period of two years is to be used in order to determine the importance of various factors.

925 Physics. Cubic Interpolation. This program has been especially written to provide a rapid and precise means of performing cubic interpolation in a table. It will be used for calculating the calibration for a platinum resistance thermometer which is given in tabular form at 1° intervals.

926 T Economics. Imports to OEEC Countries. Multiple correlation methods are to be used to determine when imports were a function of income and when they were functions of the international financial potential.

927 T Education. Reliability of Social Perception Scores. The influence of self-rating scores upon the ratings of other individuals is to be studied by statistical analysis.

928 Computer. "OR" Circuit Analysis. This program calculates the maximum and minimum values of output voltage as a function of input voltage and output current for a multiple-transistor (negative-logic) OR circuit which has diodes in series with the emitters and uses a dc level-restoring network.

929 Electrical Engineering. Electron Bunching in Single-Cavity Microwave Accelerators Operating in High-Order Modes. The purpose of this study is to obtain design criteria for single-cavity microwave accelerators. The problem

consists of solving the field equations for a cavity. The resulting equations are separable, and they may be solved by standard techniques.

Table I shows distribution of machine time for the month of January.

TABLE I

Regular Maintenance	48:01
Unscheduled Maintenance	7:06
Drum Engineering	27:49
R.A.R.	4:27
Leapfrog	80:51
Wasted	:09
<u>Use by Departments</u>	
Computer	42:20
Physics	23:14
Control Systems Lab.	32:44
Structural Research	33:04
Struct. Res. (AF 24994)	3:09
Theor. and Appl. Mech. (Task 53)	3:33
Psychology	13:35
Psychology (MD 569)	:11
Electrical Engineering	3:19
Elec. Eng. (AF 28634)	:11
Elec. Eng. (Nobsr 64723)	1:05
Elec. Eng. (AF 1406)	1:53
Chemistry	130:28
Agriculture	23:28
Mech. Eng. (ORD 1980)	:11
Ill. Dept. of Publ. Health	:54
University of Rochester	7:58
Classes	9:22
Demonstrations	:53
Miscellaneous	56:07
	556:02

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for January.

TABLE III

Memory Errors	0
Arithmetic Unit Errors	0
Input-Output Errors	2
Reader Errors	6
Punch Errors	2
Drum Errors	4
Scope Errors	3
Total	17

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
1/2/57	19:59	:01	1	(1) Probably Reader "B" error.	:00	1:08	0
1/3/57	19:58	:02	1	(1) Drum errors during drum test routine.	:00	1:20	0
1/4/57	20:00	:00	0		:00	1:40	0
1/7/57	19:59	:01	1	(1) Fifth hole error from punch "delay" feed.	:00	1:45	0
1/8/57	20:00	:00	0		:00	:46	0
1/9/57	19:48	:11	3	(1) Two different results from same tapes; reader "D" (?). (2) Two different results from same tapes; reader "D" (?). (3) Punch #5 failed to punch 2 hole.	:01	6:29	1
1/10/57	19:23	:37	3	(1) Punch #5 failing to punch 5th holes. (2) Light on Reader "B" went out. (3) Reader "D" error.	:00	1:27	0
1/11/57	20:00	:00	0		:00	3:08	0
1/14/57	20:00	:00	0		:00	8:21	0
1/15/57	19:59	:01	1	(1) Drum error during drum test routine.	:00	3:10	0
1/16/57	20:00	:00	0		:00	1:42	0
1/17/57	20:00	:00	0		:00	:49	0
1/18/57	20:00	:00	0		:00	2:30	0
1/21/57	19:58	:02	2	(1) Drum error during drum test routine. (2) Film jammed in scope camera.	:00	2:22	0
1/22/57	19:36	:24	2	(1) Drum error during drum test routine. (2) Scope circuit turned off.	:00	3:26	0
1/23/57	19:59	:01	1	(1) Film jammed in scope camera.	:00	3:34	0
1/24/57	20:00	:00	0		:00	1:02	0
1/25/57	20:00	:00	0		:00	3:14	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
1/28/57	19:47	:13	2	(1) Reader "F" failed (pin out of brake). (2) Broken lead in cannon extension plug to reader.	:00	3:32	0
1/29/57	20:00	:00	0		:00	3:10	0
1/30/57	20:00	:00	0		:00	:43	0
1/31/57	20:00	:00	0		:00	:41	0
TOTALS	438:26	1:33	17		:01	55:59	1

Reports and Seminars

Seminars

"Iterative Switching Networks," by Dr. E. J. McCluskey, Bell Telephone Laboratories, January 8, 1956.

"Formulation of the Asynchronous Circuit Problem," by Prof. David E. Muller, January 15, 1956.

Reports

Digital Computer Laboratory Report No. 76, "Coaxial Cable Memory," by Gene H. Leichner, January 10, 1957.

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*The Laboratory is sorry to report that Mr. Jerome H. Fishel was killed in an airplane accident January 20, while on Navy Reserve duty.

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

February, 1957

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and N6ori-07124, both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Design of Arithmetic Unit

The results relating to concurrent carry and borrow storage in a single register have been generalized to include all positive integral bases. We consider the ith digital position of a combination adder-subtractor with augend-minuend digit a_i, associated carry-borrow digit c_i, and addend-subtrahend digit m_i. The index i increases with decreasing significance of the digital position. The digit a_i has the values 0, 1, ..., r-1 where r is the base. The associated carry-borrow digit c_i has the values -1, 0 or +1, with the restrictions that

a) if $c_i = -1$, $a_{i+1} = r - 1$

b) if $c_i = +1$, $a_{i+1} = 0$.

The digit m_i has the values 0, 1, ..., r-1 for addition and 0, -1, ..., -(r-1) for subtraction.

For a consistent system, it must be shown that sum-difference digits s_i and associated carry-borrow digits b_i can be generated such that

a) if $b_i = -1$ $\quad s_{i+1} = r - 1$

b) if $b_i = +1$ $\quad s_{i+1} = 0$.

Otherwise the s_i can have the usual values 0, 1, ..., r-1.

We view the formation of s_i and b_i as consisting of two successive digitwise additions. We first form the sum $s_i' = a_i + m_i$ and note that $0 \leq s_i \leq 2r-2$ for addition and $-(r-1) \leq s_i' \leq r-1$ for subtraction, for each i. In either case s_i' can be represented as a carry-borrow $K_{i-1} = -1$, 0, or +1 and a digitwise sum s_i'' having the values 0, 1, ..., r-1. The carry-borrow c_{i-1} is preserved by forming $K_{i-1}' = K_{i-1} + c_{i-1}$. It is shown below that

$K'_{i-1} = 1, 0,$ or $+1$. A second addition of s''_i and K'_i yields a result x_i in the range $-1 \leq x_i \leq r$, which is represented by digits s_i and b_{i-1} having the desired properties.

The implications of the restrictions on s_i and b_{i-1} (or on a_i and c_{i-1}) are these:

1) A single binary storage device can be used for any one carry-borrow digit b_{i-1} (or c_{i-1}). The values 0 and r-1 of s_i (or a_i) are easily distinquishable and can be used to determine the sign of a non-zero b_{i-1} (or c_{i-1}).

2) The restrictions simplify the formation of the intermediate carry borrow K'_{i-1}. If $c_{i-1} = +1$, then $a_i = 0$ and $s'_i = m_i$. Therefore for addition $K_{i-1} = 0$ and $K'_{i-1} = c_{i-1} = +1$, and for subtraction if $m_i < 0$ $K_{i-1} = -1$ and $K'_{i-1} = 0$. On the other hand, if $c_{i-1} = -1$, then $a_i = r-1$. For addition, if $m_i > 0$, $K_{i-1} = +1$ and $K'_{i-1} = 0$, and for subtraction $K_{i-1} = 0$ and $K'_{i-1} = c_{i-1} = -1$.

Two versions of an adder with separate carry storage were designed for operation in base 4. The first version was designed in accordance with the theory outlined above. The second version can most easily be described as a modified binary adder with the carry chain broken at alternate binary digital positions. The carry restriction that $c_{i-1} = 1$ implies $s_i = 0$ holds for the base 4 digit s_i in the former version. In the modified binary version, only the adjacent <u>binary</u> digit is necessarily zero. Assimilation circuits for the two versions have not yet been designed. Base 4 operation (either of the above versions) would have an advantage over the binary design in that only half as much equipment would be required for carry storage and transfer.

2. High-Speed Circuits

Flipflop circuits similar to those in Report 77 are being considered with output voltages of ± 2v. If this can be done, it will be possible to carry the logic through several stages without signal standardization.

Some last few transistor flipflop designs were tried using Routines #719 and #819. All the designs found which are reasonable require 20 ma circuits, $\pm 3\%$ tolerance on power supplies, and dc α's of $0.93 \rightarrow 1.00$ -- that is, pick transistors with dc α's in the range of $0.95 \rightarrow 1.0$ and allow for a drift of from 0.95 to 0.93. Further, all the designs require a diode on the collector of the flipflop transistor to keep it out of saturation. The resistances of the collector resistor and the resistor which drives the base of the opposite

transistor are around 1K. Then a ±3% resistor tolerance can be obtained if 30 volt supplies are used and only 0.5 ma load current is desired, or a ±2% resistor tolerance must be used if 1.0 ma load currents are desired with 30v supplies, or if 25v supplies are desired for only 0.5 ma load currents.

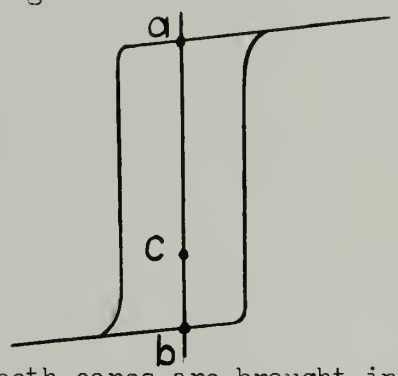
An EXCLUSIVE OR circuit and a complement gate circuit for use with the ±2v levels are being designed.

3. Memories

Proposed 1.5 μsec Core Memory

Experimental tests on various aspects of the core-memory design have been continued throughout the month. An experimental one-word memory is nearing completion. It differs from the design referred to as Memory Design 2 in the November report, chiefly by incorporating the idea of "partial switching," described below. The possibility of modifying the proposed memory so that four words would be read (or written) simultaneously is also being considered.

The idea of "partial switching" can be explained with the aid of the diagrammatic hystersis loop shown. Two cores A and B are used to represent one bit, and according to the original plan a "1" might be represented by core A in state a and core B in state b, and a "0" by core A in state b and core B in state a. In either case the read-pulse would bring both cores to state b, causing an output pulse the sign of which would depend on whether a "0" or "1" was stored. The write-pulse would then bring either core A or B back to the state a.



Provided that both cores are brought into the same state, b, by the read-pulse it is not necessary that the write-pulse bring one core all the way to a. Some intermediate value of magnetization such as c would do as well. The amount of energy required to switch to c instead of a is much less, reducing heating

effects, and also less time is needed to switch to c than to a. The exact improvement in these respects cannot be calculated accurately since exact calculations can only be made for cores completely switched by constant current pulses.

The simplest way to provide for partial switching is to reduce the size of the switch core. Since the switch core is linked to the memory cores by a low resistance loop, the flux change in the memory cores is approximately equal to the flux change in the switch cores. The connecting loop, however, has some resistance and this resistance, though small, leads to some difficulty in making sure that the read-pulse always brings both cores to the state b. This point will be checked by tests on the one-word memory.

Small-Size Working Memory

The balance of memory and arithmetic unit of the machine indicates strongly the need for a memory with an access time comparable to that expected for an addition time. For this purpose a memory of about 64 words with an access time of 0.1 or 0.2 μs would be desirable. Some preliminary considerations have been made of using a Williams memory or a diode capacitor memory for this kind of use. The Williams memory, because the number of bits stored would be much smaller than usual per cathode ray tube, would have no read-around problem but coupling between the deflection plates and the pickup screen would certainly be a problem. The diode capacitor memory would in principle be a satisfactory solution, but the drive amplifiers (128 for a 64-word memory) would need to be able to furnish about 750 ma per amplifier. Some further considerations are being given to each of these types of memories and a more detailed design of the diode capacitor memory is being worked on.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. A paper on the theory of asynchronous circuits has been prepared by combining Digital Computer Laboratory Reports 75 and 78. It will be described briefly at the International Symposium on the Theory of Switching to be held at Harvard University April 2-5, and will appear in full in the proceedings of the conference, which will be published early in 1958.

This paper treats the theory of asynchronous circuits in a mathematically rigorous way. Much of the theory is concerned with "semi-modular" circuits which are shown to be speed-independent in the sense that the ultimate behavior of such circuits is independent of the speeds of the logical elements which make them up. The states of such a circuit may be related to vectors, whose components are non-negative integers. These vectors, called C-states, form a semi-modular lattice with a zero under numerical partial ordering. Numerical partial ordering of the C-states is shown to correspond to the chronological ordering of the states. This lattice of C-states describes the possible modes of behavior of the circuit in a way which is more amenable to analysis than do the states themselves.

The remainder of the paper is concerned with three aspects of the semi-modular circuit problem, all of which are treated by considering the lattice of C-states. They are the following:

a) Periodicities in the lattice of C-states are classified and are shown to correspond to cyclic changes taking place in the circuit.

b) Ideals of the lattice are related to sets of signals which might be apparent to an observer who had only limited access to the circuit.

c) The implications of restricting ones consideration to distributive lattices are considered. This investigation, which was finished this month, is described in section 2.

2. The theory of distributive circuits is important because of a general synthesis technique which is used to produce distributive circuit designs.

The following three assumptions were shown to be equivalent.

a) The lattice of C-states is modular.

b) The lattice operations for forming the greatest lower found and least upper bound are componentwise minima and maxima respectively.

c) The lattice of C-states is distributive.

If the lattice of C-states possesses these properties, the corresponding circuit is said to be distributive. Since the lattice of C-states satisfies the descending chain condition it is uniquely determined by its join-irreducible elements, provided their ordering is given. The set of join-irreducible elements was shown to be isomorphic with a certain set of ideals called C-signals which may be specified by means of two integers; one integer equals the number of changes which have occurred at a given node in the circuit and the other is the node number. Inclusion among the C-signals defines a causation relation among the changes taking place within the circuit which uniquely determines the lattice of C-states if it is distributive. Thus, the partially ordered set of C-signals may be taken as the starting point for circuit synthesis. A rule for determining whether a given element is excited or in equilibrium is set down and from this rule one may place suitable restrictions on the functions which define the circuit, provided the circuit uses binary signals.

Thus, from a listing of the changes taking place in a circuit and the causation relationships between them, one may design the corresponding circuit and since it is distributive it must be speed-independent. Future work along this line will be directed toward determining what restrictions must be placed upon the set of C-signals to make the circuit realizable.

3. Work is progressing in the design of speed-independent control and arithmetic circuits of the type which may be used in the high-speed computer. The purpose of this study is to determine whether the present synthesis techniques are adequate for designing circuits of the complexity required by the computer. Speed independent designs have been achieved for a Robertson-Metze adder and carry assimilator.

PART III

MATHEMATICAL METHODS

1. Programming. (Supported by Office of Naval Research under Contract N6ori-07130.)

A new program has been written for storing library routines on the drum, so that they may be used in conjunction with the symbolic address routine. To date, the following routines have been stored on the drum and are available for use by programmers: P-16, Y-1, R-1, S-4, T-4, T-5, F-1, S-5, and N-12. These routines include an input routine, a print routine, a drum transfer routine, a routine for solving differential equations, and routines for evaluating exponential functions, trigonometric functions and logarithms.

A combined post mortem routine has been written and placed on the drum. It contains facilities for printing words as integers, fractions, order pairs, or in sexadecimal or floating decimal form. These words may be taken from either the Williams memory or the drum. An improved address search routine is also included. To use these routines, one need only input short sections of tape specifying the nature of the printout and the locations to be printed.

The multiple regression routine, K-12, has been modified in order to allow one to transform the random variables being used. Function routines available for the transformation are the following: 0, X, X^2, X^3, log X, $\sin^{-1} X$, $\sqrt{X}$. As many as 50 variables can be read into the machine, but the capacity is still 22 non-eliminated variables, as before.

2. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

N-12 (225) Infraput. This versatile input routine may be used to read and store sequences of either fractions or integers. As many as twelve decimal digits may be punched for each fraction and in all cases the closest binary approximation to the punched fraction is obtained. Routine N-11 has been superceded by the present routine which has a sufficiently fast inner loop to yield maximum reading speed. All of the earlier fraction input routines are about twice as slow with the existing reader control.

N-13 (226) Input a Sequence of Fractions All Having the Same Number of Decimal Digits. This routine has the same speed and accuracy as N-12, but lacks its versatility. It should be used in place of N-12 only when it is necessary to conserve space in the Williams memory.

N-14 (227) Input a Sequence of Integers. As in the case of N-13, this routine possesses the speed of N-12, but lacks its versatility and is to be used only if no fraction input routine is required and space must be conserved.

S-5 (231) 1/32 Natural Logarithm. This routine is to replace the earlier logarithm routine, S-1. By improved programming, the present routine was made 9 words shorter and 8 times as accurate as S-1.

M-19 (232) Solution of the Matrix Equation $Ax = \lambda Bx$, where A and B are Symmetric and B is Positive Definite. This routine supercedes M-5 and differs from it in the following respects.

1. An error in M-5 was corrected in the present routine.
2. A faster input routine is used with M-19.
3. The eigenvalues and eigenvectors of B may also be printed using M-19.
4. Several programmed checks are incorporated in M-19.
5. The maximum order of the matrices was increased from 17 to 19.

3. Analytical Program. (Supported by National Science Foundation under Grant G-2794.)

The solution of the Einstein field equations for a static spherically symmetric distribution of a perfect fluid have been reduced to the solution of the set of three ordinary differential equations:

$$\Phi_R = \frac{1}{2} \frac{R^3 P + M}{R^2 - MR}$$

$$M_R = (\Sigma - P)R^2$$

$$P_R = -\Sigma\, \Phi_R \quad ,$$

where R is a dimensionless variable related to the radial distance, P is a dimensionless variable related to the pressure and Σ - P is a dimensionless representation of the total energy density per unit volume (the mass density plus the internal energy density). The line element of space time is given by

$$ds^2 = e^{2\Phi}\, dt^2 - \frac{1}{c^2}\, e^{2G}\, dr^2 - \frac{1}{c^2}\, (d\theta^2 + \sin^2\theta d\phi^2),$$

with

$$e^{-2G} = 1 - \frac{M(R)}{R}$$

Numerical integrations of these equations will be carried out for various kinds of fluids, that is, various assumptions will be made regarding the dependence of the quantity Σ - P as a function of P and R and numerical solutions of the system of differential equations will be determined subject to the conditions:

$$\Phi(1) = \frac{1}{2} \log(1 - M(1))$$

$$P(1) = 0$$

$$M(1) < 1 \ ,$$

with

$$0 \leq M(R) < R$$

for all R in the interval

$$0 \leq R \leq 1 \ .$$

The conditions at R = 1 are obtained from the requirement that the line element given above match with the Schwarzschild exterior solution at R = 1. If M(R) satisfies the condition given above, then the solution will be non-singular in the region occupied by the matter.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During February specifications were presented for 18 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 930. Numbers followed by T are for theses.

930 Computer. Modification of Library Routine Y-3. Library Routine Y-3 is a routine to place library subroutines on the drum in compacted form so that they may be called for by means of special directives on a tape. This rewritten version permits these library routines to be used in conjunction with the Symbolic Address Decimal Order Input.

931 Sociology and Anthropology. This study is concerned with gauging effects of a mentally retarded child on family integration under various conditions. Factors taken into account are age and sex of the retarded child, the presence of brothers and sisters, socio-economic status of the parents, contact between the family and neighbors, friends, grandparents of the child, the degree of mental retardation of the child, the amount of interaction with the child, and institutionalization of the child. The aim of the study will be to add to sociological knowledge of families in crisis and provide information for parents and social workers dealing with the mentally retarded.

932 Student Counseling Bureau. Freshman Reading Study. This study is designed to secure information concerning the relations of reading abilities to other tests used in the regular Freshman Guidance Battery which is used by the Student Counseling Bureau at Navy Pier Branch in Chicago.

933 Theor. and Applied Mech. Tool Settings for Pressure Vessel Models. It is desired to compute transversal and longitudinal settings of a cutting tool in a lathe for machining photoelastic models of pressure vessels, using a tool feed of about 1/100 inch.

934 Mathematics. Self-Gravitating System Orbits. The problem consists of solving ordinary differential equations describing the motion of a particle in a time-varying field of forces.

935 Physics. Influence of the Pauli Principle on the Motion of Electrons in a Superconductive Media. The program will find that superposition of free electron states having momentum greater than $k_o h$ which gives the lowest total energy. The purpose of this investigation is to determine whether properties associated with superconductivity will appear in this system.

936 Structural Research. Moments M_y and M_x in a Simply-Supported Plate due to a Moment Applied at One Edge. The present program evaluates the expressions for the moments in a simply-supported panel of a plate subjected to a sinusoidally varying moment along one edge.

937 Civil Engineering. Grain Size Distribution of Soils. This problem involves the computations required to determine the grain size distribution of mixed-grained and fine-grained soils. The basic data are obtained from a sedimentation analysis in which the density of the suspension is determined at various time intervals by means of a hydrometer.

938 T Aeronautical Engineering. Incompressible Non-viscous Flow. The problem consists of investigating incompressible non-viscous flow around a delta wing with attached vortex sheets.

939 T Electrical Engineering. Frequency Modulation Response to an Electrical Network. A step change of frequency is applied to the input of an electrical network. The program determines the frequency as a function of time at the output of the network.

940 Physics. Photoproduction Cross Sections. A formula is used to evaluate the differential cross-section for single meson production in deuterium by gamma rays, as a function of gamma ray energy and pion momentum at four angles.

941 Computer. Givens' Method for Finding Eigenvalues. This routine for finding eigenvalues of a symmetric matrix by Givens' method will eventually be placed in the Illiac library.

942 T Agricultural Economics. Economic Analysis of Non-tillable Pasture Renovation. The productivity of tillable and non-tillable land on farms in Western Illinois will be compared using standard statistical techniques.

943 Psychology. Prediction of Military Dicipline. The tendency of students at West Point to obey rules and regulations is correlated with their scores on certain perception tests.

944 Inst. of Comm. Research. Southwest Project on Psycholinguistics. Subjects from five different cultures, Southwest Spanish, Zuni, Hopi, Tewa and Navaho Indians, described a series of concepts on 15 semantic differential scales. Analysis is aimed at comparing the relations among the scales produced by the five groups, the hypothesis being that the interrelations among the scales are essentially the same.

945 Structural Research. Analysis of Rectangular Orthotropic Plates. This study is concerned with the analysis of a rectangular orthotropic plate, fixed along three edges and free along the fourth. The effects of a uniform load and of a linearly varying load on such a plate are analyzed for various of aspect ratio and ratio of rigidities.

946 T Economics. Relation of Stock and Bond Yields in the Postwar Period. Two classes of stocks and two classes of bonds were studied to determine relations between yield and risk.

947 Michigan State University. Eigenvalue Practice Problem.

Table I shows distribution of machine time for the month of February.

TABLE I

	Hrs.:Min.
Regular Maintenance	34:48
Unscheduled Maintenance	6:58
Drum Engineering	35:02
R.A.R.	5:48
Leapfrog	74:44
Wasted	:10

Use by Departments

Computer Group	22:58
Physics	14:17
Control Systems Lab.	33:26
Structural Research	8:43
Struct. Res. (AF 24994)	7:30
TAM (Task 53)	2:04
Psychology	41:04
Elec. Eng.	8:46
Elec. Eng. (AF 1406)	4:24
Elec. Eng. (Nobsr 64723)	7:55
Chemistry	111:38
Elec. Eng. (AT 392)	1:36
Agriculture	15:32
Mech. Eng. (ORD 1980)	:36
Demonstrations	1:31
Miscellaneous	40:30
	480:00

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted

to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for February.

TABLE III

Punch Errors	2
Reader Errors	4
Memory Errors	1
Scope Errors	1
Input-Output Errors	1
Drum Errors	8
Total	17

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
2/1/57	19:45	:15	2	(1) Punch No. 5. Gate "B" bad (2) Punch No. 5. Gate "B" bad	:00	1:44	0
2/4/57	19:16	:44	1	(1) Drum failure (Drum Test Code).	:00	:58	0
2/5/57	19:19	:41	2	(1) Drum failure (During solution of problem) (2) Drum failure (Drum Test).	:00	3:13	0
2/6/57	19:39	:21	2	(1) Drum failure (Drum Test). (2) Output switch (Input-Output rack)	:00	4:34	0
2/7/57	20:00	:00	0		:00	2:40	0
2/8/57	18:21	1:30	1	(1) Scope error.	:09	2:26	0
2/11/57	18:53	1:06	1	(1) Memory error pos 2^{-36}	:01	5:30	1
2/12/57	20:00	:00	0		:00	2:15	0
2/13/57	20:00	:00	0		:00	4:15	0
2/14/57	19:59	:01	1	(1) Drum failure (Drum Test).	:00	2:00	0
2/15/57	20:00	:00	0		:00	1:34	0
2/18/57	19:53	:07	1	(1) Reader "B" error	:00	4:16	1
2/19/57	20:00	:00	0		:00	1:16	0
2/20/57	20:00	:00	0		:00	:58	0
2/21/57	19:53	:07	4	(1) Reader error. Brake on "K" failed. (2) Drum failure. (Drum Test). (3) Drum Failure. (During solution of problem) (4) Drum Failure. (During solution of problem)	:00	4:04	0
2/22/57	19:58	:02	2	(1) Reader "F" failure (2) Reader "K" failure	:00	2:30	0
2/25/57	20:00	:00	0		:00	1:32	0
2/26/57	20:00	:00	0		:00	:59	0
2/27/57	20:00	:00	0		:00	5:10	0
2/28/57	20:00	:00	0		:00	4:47	0
TOTALS	394:56	4:54	17		:10	56:41	2

Reports and Seminars

Seminars

"Overflow Analysis for an Arithmetic Unit with Separate Carry Storage", by Prof. James E. Robertson, February 12, 1957.

"Machine Translation of Languages", by Algirdas A. Avizienis, February 19, 1957.

"An Iterative Method for Solving Linear Equations", by Gene H. Golub, February 26, 1957.

Reports

Digital Computer Laboratory Report No. 77, "Computer Circuits with 30 Millimicrosecond Operation Times", by Gene H. Leichner and John L. Muerle, February 6, 1957.

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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

March, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Design of Arithmetic Unit

The logical design of a binary adder-subtractor with coincident carry-borrow storage was completed, together with the logical design of the carry-borrow assimilator.

It seems practical to split the logic of the adder with separate carry storage into two parts such that the operation of addition without carry assimilation is performed in two steps. This tends to balance the distribution of the logical circuitry and should lead to a decrease in operation times for speed-independent circuits. Further investigations are planned.

2. 1.5 Microsecond Memory

A one-word memory intended to test some features of the operation of a word arrangement memory described earlier has been completed. This memory has the following properties:

a) 50 digits: 50 digit cores + 50 compensating cores,

b) 1 word: 1 switch core composed of 24 S-3 digit cores,

c) 2 possible states: 1. 010101.....
2. 101010.....,

d) 3 possible cycles: 1. Word #1 recycled continuously
2. Word #2 recycled continuously
3. Word #1, Word #2, Word #1, etc.

This one-word memory, along with its driving and logical equipment, has been built and tested, and performs very well in both states and in all three cycles. Tests have been made showing these characteristics:

1) Read time 0.4 μsec#
Write time 0.4 μsec

2) Read $\begin{cases} \text{Drive current} = 1.3 \text{ amp.} \\ \text{Bias} = 0.6 \text{ amp.} \end{cases}$

Write - exhibit current = 0.4 amp.

3) Peak output voltage per core pair = 0.2 volt.

#These times are minimums and are exclusive of all decoding and gating times. A 4096-word memory would need 0.6-0.8 μsec. more for these functions.

The signal-to-noise ratio is at least 10 to 1.

Attempts will be made with this memory to reduce the drive to the bit cores thereby preventing the bit cores from reversing fully. Any success in this direction will reduce cycle time and core heating.

3. Arrangement and Control

One possible logical arrangement for the new computer has been considered in some detail and described in File No. 213: "Control" by D. B. Gillies and J. P. Nash, March 8, 1957. For definiteness, the following sizes and speeds were taken:

Core memory	4096 40-bit numbers	1.5 μsec
Fast memory	64 words	.1 μsec
B-registers	7 12-bit registers	
Arithmetic unit	2 single-length connected shifting registers	
B-line adder		
Extra instruction registers	2, shorter than 20-bit, for the purpose of saving requests for core memory data.	

Simultaneous 4-word transfers were assumed between the two memories for two reasons:

(a) to increase the channel rate of flow of information, and

(b) to reduce the number of transfer instructions.

A data transfer consists of one 4-word block whereas an instruction transfer consists of two 4-word blocks (because two transfers can be done during one multiplication). Data and instructions are used via the fast memory--no operands go directly from the core memory to control or the arithmetic unit. The 64-word fast memory is addressed by two octal digits DE. If D = 0, 1, 2 the address E is not B-modified. If D = 3, 4, 5, 6, 7 the least significant 3 bits of B3, B4, ..., B7 respectively are added to

E mod 8 to produce an octal digit E' and the modified address is DE'. Normally B3, B4, ... contain core-store addresses, and this modification system allows

(a) addressing of the operands in either memory,

(b) a great reduction in the number of bits in an instruction,

(c) (optional) anticipatory reading of the next block or writing of the last block.

In this design, memory transfers occur while the arithmetic unit is busy--particularly during multiplication and division, and the computer saves up requests for data to be executed during this time. In problems with a high density of multiplication it appears to work quite well, and in problems with no multiplication at all, the simultaneous multiple-word transfer facility increases the speed of operation, especially of instruction accesses.

4. High-Speed Circuits

A half-adder circuit with an operation time of 36 mμs using the GA-53233 transistor has been designed. It is described in File No. 216.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. A method for synthesizing distributive circuits is being studied which takes the partially ordered set of C-signals as its starting point. Each C-signal is specified by two integers: a node number and a number indicating how many signal changes have occurred at the given node since the circuit was placed in its initial state. Ordering relations between the C-signals represent causation relationships between the changes taking place in the circuit.

Given a partially ordered set of integer pairs, one may write restrictions to be placed on the functions representing a binary circuit. If these restrictions are not inconsistent they are sufficient to ensure that the set of integer pairs correspond to a possible set of C-signals and that the resulting circuit will carry out the operations defined by this set of C-signals. Furthermore, the resulting circuit will be distributive with respect to the given initial state, and consequently speed-independent.

The object of the present investigation is to determine another way of expressing the above condition that a given partially ordered set of integer pairs should correspond to a set of C-signals. This problem has not been completely solved. So far restrictions have been found which are necessary and sufficient that a given set of integer pairs will generate a set of numerical vectors which form a distributive lattice with a zero under the operations of forming numerical maxima and minima. These restrictions are therefore necessary for the set of integer pairs to represent a set of C-signals. Similarly, restrictions on the set of numerical vectors have been found which are necessary and sufficient for the generation of the corresponding set of integer pairs. Further restrictions on the set of integer pairs are now being sought which will ensure that a corresponding circuit may be synthesized.

2. Preliminary designs were completed and checked for a shift counter and a system for either shifting or assimilating carries, dependent upon a given signal. Such a system may be extended to take care of the problem of doing any of several operations depending on a given signal.

Logical designs for a self-checking flipflop have been achieved, which will permit the elimination of flipflop clearing in the design of speed-independent circuits.

Work was also begun on the problem of sensing circuits, in connection with the selection problem discussed above.

The main routine for testing the circuits was revised by inserting black switch stops and line feed prints to make the code more convenient to use.

PART III

MATHEMATICAL METHODS

1. Numerical Analysis. (Supported by Office of Naval Research under Contract N6ori-07130.)

An iterative method for solving the system of n linear equations

$$Ax = b$$

where A is a symmetric n x n matrix, and x and b are n component vectors is being studied numerically. At present A is chosen to be a matrix related to a difference operator approximating the differential operator $\frac{d^2}{dx^2}$. The iteration formula being used is

$$\eta_{k+1} = 2b_k \left[\frac{2}{\alpha+\beta}(b-A\eta_k) + \eta_k - \eta_{k-1}\right] + \eta_{k-1},$$

$$\eta_0^i = 0, \eta_1 = 1$$

where α and β are the smallest and largest proper values of the matrix A respectively and the numbers b_k are defined by the iterative relations

$$b_{k+1} = \frac{1}{2-(1-\epsilon)^2 b_k},$$

$$\epsilon = \frac{2\alpha}{\alpha+\beta},$$

$$b_0 = 1.$$

This iteration formula is equivalent to one given by Stiefel who studied the behavior of the residuals defined by

$$r_k = A\eta_k - b.$$

It is also that given in an unpublished manuscript by von Neumann who studied the nature of the convergence of the η_k to the true solution x.

The numerical experiments being planned will throw some light on the behavior of the errors as a function of the number of iterations and the parameter ϵ. It is hoped that one will be able to study the effects of round-off for a broad class of matrices.

2. Flows Behind Shocks. (Supported by National Science Foundation under Grant G-2794.)

Coding of the integration of the flow equations behind a shock is nearly completed. Except for the iteration procedure for obtaining the Cauchy data on the shock given a streakline, the subroutines involved in the problem for a given streakline and those involved in the problem for a given shock are identical. The latter case will be handled first in order to get some feeling for the behavior of the solutions without the additional complication of the iteration and to provide some data for testing the latter case.

3. Analytical Program. (Supported by National Science Foundation under Grant G-2794.)

A paper entitled "The Fundamental Solution of a Linear Parabolic Equation Containing a Small Parameter" has been completed. The main results are the following. Consider the equation

$$L_\epsilon(u) \equiv \epsilon \sum_{i,j=1}^{n} a_{ij}(x,y)\, u_{x_i x_j} + \sum_{i=1}^{n} a_i(x,y)\, u_{x_i} + b(x,y)\, u - u_y = 0,$$

where $\epsilon > 0$ is a parameter, the matrix $(a_{ij}(x,y))$ is symmetric and positive definite, and where $a_{ij}(x,y)$, $a_i(x,y)$, $\dfrac{\partial a_i(x,y)}{\partial x_j}$, $b(x,y)$ are uniformly bounded, uniformly continuous, and satisfy a uniform Hölder condition with respect to x for all $x = (x_1, \ldots, x_n)$ in E^n and all y in $[y', y'']$. The fundamental solution of $L_\epsilon(u) = 0$ is shown to exist under these conditions and a parametrix representation valid for all $\epsilon > 0$ is given. Moreover, if $u(x,y)$ is the solution of the initial value problem

$$L_\epsilon(u) = 0 \text{ for } y' < y \leq y'', \; u(x,y',\epsilon) = g(x),$$

where $g(x)$ is a given uniformly continuous and bounded function, then for $y > y'$

$$\lim_{\epsilon \to 0+} u(x,y,\epsilon) = v(x,y)$$

exists uniformly in x and $v(x,y') = g(x)$. $v(x,y)$ is a generalized solution of the initial value problem.

$$L_0(w) = 0 \text{ for } y' < y \leq y'', \; w(x,y') = g(x),$$

and if $b(x,y)$ and $g(x)$ have continuous and uniformly bounded first partial derivatives with respect to x it is an actual solution.

A generalization of these results to linear parabolic systems is being investigated.

4. Programming.

New Eigenvalue Program: A program is being prepared for finding the eigenvalues of a symmetric matrix using a method of Givens. There are two parts to the calculation. In the first part, the matrix is rotated to make it assume a tri-diagonal form in which all the off-diagonal elements are zero except those adjacent to diagonal elements. This is accomplished in significantly fewer steps than are required by the Jacobi process now in use, which uses repetitive rotations to reduce the matrix to diagonal form. In the second part of Givens' process the eigenvalues are obtained from the reduced matrix by a binary chopping method which depends upon the calculation of a Sturm sequence.

The magnetic drum is used to hold a triangular matrix representing the original symmetric matrix. Matrices as large as 128X128 can be handled in this way. During rotation it is necessary to transfer both rows and columns of this matrix back and forth between the drum and Williams memory. The transfer time for both rows and columns is minimized by storing the matrix elements in such a way as to take advantage of the fact that electronic switching between tracks on the drum is accomplished without delaying access.

Symbolic Address Routine: A preliminary report was written on the new symbolic address routine and further progress was made in the preparation of the routine. This rewritten version will contain facilities which are not in the present routine and will be considerably faster.

5. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

K-14 This program is a major revision of the earlier multiple regression routine K-12. The new routine permits the user to apply any one of seven transformations to the variables before carrying out the analysis. It also permits one to use as many as 50 variables while the older routine was restricted to not more than 22.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During March specifications were presented for 18 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 948. Numbers followed by T are for theses.

948 Computer. Sorting by Merging. This program was prepared to investigate techniques of sorting by merging.

949 T Education. Comparison of Judges' Ratings of Dimensions derived from Spherical Objects. A statistical analysis will be made of the lack of objectivity of judges in estimating physical properties of balls attached to strings.

950 Psychology. Pilot Study Investigating Simple Structure. It is proposed to study the subjective oriteria for determining whether or not a given factor matrix may be rotated to yield a good simple structure. This will be done by comparing the results of rotating random matrices with the results obtained by rotating actual factor matrices which are thought to have a good simple structure.

951 Quartermaster Food and Container Institute. Factor Analyses of Odor and Food Preferences. Various statistical analyses are to be performed on data obtained in a study of food preferences in the Armed Forces.

952 T Music and Education. An Investigation of Relationships of Student Teacher Satisfaction and Cooperating Teacher Traits. In general, the present investigation is concerned with the relationship of item and total scores obtained on a "Student Teaching Inventory" (dependent variable) and (1) eleven personality factor scores obtained on the Cattel Music Preference Test of Personality, (2) the total score on the Minnesota Teacher Attitude Inventory, (3) three part-scores and total score on the Aliferis Music Achievement Test, (4) two scores obtained on the Strong Vocational

Interest Blank. These four types of scores will serve as independent measures. Multiple correlation of these measures with the dependent measure will be the object of analysis.

953 T Control Systems Lab. High Speed Digital Shift Register. The problem is to study the characteristics of and to build a high speed digital shift register. The equations describing its behavior are non-linear and require numerical solution.

954 Electrical Engineering. Investigation of Pole-zero Shift in Driving point Impedance of Ladder Network with Changes in Circuit Elements (Root Locus). This program will be used to compute the driving point impedance and the positions of poles and zeros of the driving point impedance for a general ladder network. An investigation will be made of the shifts of poles and zeros which occur when the circuit elements are changed.

955 T Aeronautical Engineering. Dynamic Stability Analyses (Aircraft). A 5-degree of freedom dynamic stability analysis of an airplane will be made. The altitude and speed are fixed. The resulting five differential equations will be solved by standard techniques.

956 T Structural Research. Stress and Strain due to Concentrated Forces. The general purpose of this study is to evaluate the effect of transient and static wheel loads on airfields. This program will calculate the stress and strain due to concentrated load on an elastic infinite plate supported by a semi-infinite elastic material.

957 Economics. Underwriting Expenses. This program will study the relationships between known measurable characteristics of property insurance operations and levels of costs of these operations.

958 Physics. Ground State of Tritium Nucleus. This program will solve the Schroedinger equation for the tritium nucleus ground state. Methods similar to those used on the helium problem will be employed here, since the only essential difference is the potential energy.

959 Institute of Labor and Ind. Relations. Factor Analysis of Union-Management Data. This is an attempt to apply quantitative dimensional analysis to a set of data on important aspects of the union management relationship in 41 different Illinois companies.

960 Structural Research. Moments in a Simply Supported Panel Due to a Deflection Applied at One Edge. The present program evaluates the expressions for the bending moments in a simply-supported panel of a plate subjected at one edge to a sinusoidally varying deflection without rotation.

961 Computer. Iterative Solutions of Linear Equations. This program will use an iterative method for solving systems of linear algebraic equations. The method, due to von Neumann, carries out a calculation which produces the same sequence of approximates as that produced by the method of Stiefel. Iterative methods are most useful for sets of equations having many zero coefficients.

962 T Phys. Chem. Calculation of the Proton-Proton Coupling Constant in Methane. This program, which calculates the proton-proton, nuclear spin-nuclear spin coupling for methane requires a calculation of the coefficients of the various states which contribute to the ground states of the wave function. These are obtained as eigen-vectors of a matrix equation. The matrix elements are taken as functions of some rather uncertain energy parameters.

963 Agriculture. 4-H Keeping Fit Data - Analysis Variance. This program will be used to set up standard score tables for determining the level of fitness of 4-H boys and girls. An analysis of variance is to be made of several variables such as age and body type.

964 Agronomy. Calculate Munsell Color Index. Reflectance readings for 31 wave lengths are made in each of several fruits. From these reflectances a set of 3 Munsell color indexes are calculated to determine the exact color.

965 Civil Engineering. Propagation of Brittle Crack. The problem under investigation is the dynamic propagation of a "brittle" crack through materials which are usually

assumed ductile. At present the investigation of this problem includes laboratory tests of large plate specimens and analytical studies from which it is hoped an explanation of this type of fracture may evolve. This program will compute strain values as a function of time from experimental measurements.

Table I shows distribution of machine time for the month of March.

TABLE I

	Hrs:Min.
Regular Maintenance	42:59
Unscheduled Matinenance	15:30
Drum Engineering	35:27
R.A.R.	7:41
Leapfrog	63:29
Wasted	:00
<u>Use by Departments</u>	
Computer	22:22
Physics	26:05
Control Systems Lab.	54:05
Structural Research	23:03
Struct. Res. (AF 24994)	5:02
Struct. Res. (AF 3203)	:14
Theor. and Appl. Mech. (Task 53)	:23
Psychology	27:03
Electrical Engineering	19:14
Elec. Eng. (AF 28634)	:09
Elec. Eng. (Nobsr 64723)	17:25
Elec. Eng. (AF1406)	1:20
Elec. Eng. (AT 392)	9:11
Chemistry	60:20
Agriculture	25:01
Mech. Eng. (ORD 1980)	:19
Quartermaster Food Institute	:43
Institute of Communications Research	1:46
Classes	15:47
Demonstrations	16:20
Miscellaneous	27:50
	518:48

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for March.

TABLE III

Punch Errors	6
Reader Errors	1
Memory Errors	1
Scope Errors	5
Drum Errors	5
Arithmetic Errors	1
Unknown Errors	3
* Miscellaneous	1
Total	23

* Fan belt in air conditioner broke.

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
3/1/57	19:59	:01	1	(1) Reader error "F"	:00	6:29	0
3/4/57	19:59	:01	1	(1) Unknown	:00	6:50	0
3/5/57	20:00	:00	0		:00	1:54	0
3/6/57	19:15	:45	1	(1) Drum error	:00	1:05	0
3/7/57	19:59	:01	1	(1) Unknown	:00	1:06	0
3/8/57	19:59	:01	1	(1) Drum error	:00	1:21	0
3/11/57	19:57	:03	1	(1) Scope error	:00	3:34	0
3/12/57	19:10	:50	3	(1) Arithmetic error. (2-27 R III - exact trouble not found) (2) Memory error. (S. C. Restorer 6ALS envelope broke - mem. pos. 2-13) (3) Drum error	:00	2:50	2
3/13/57	16:22	3:38	1	(1) Scope error (TSP=1 not going negative enough)	:00	2:14	0
3/14/57	19:46	:14	3	(1) Unknown (2) Punch #1 failed to punch a 1 hole (3) Punch #1 failed to punch a 1 hole	:00	:58	0
3/15/57	20:00	:00	0		:00	:46	0
3/18/57	19:52	:08	1	(1) Tape jammed in punch #4	:00	:45	0
3/19/57	19:45	:15	2	(1) Punch error #4 (2) Scope error	:00	1:28	0
3/20/57	19:59	:01	1	(1) Scope error (Gate "4" C. F. Cathode resistor opened up)	:00	:45	0
3/21/57	19:59	:01	1	(1) Drum error	:00	4:16	0
3/22/57	19:19	:41	2	(1) Scope error (2) Drum error	:00	:52	0
3/25/57	20:00	:00	0		:00	:48	0
3/26/57	19:30	:30	1	(1) Punch error #5	:00	3:30	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
3/27/57	19:44	:16	1	(1) Punch error on Leapfrog #5	:00	3:06	1
3/28/57	20:00	:00	0		:00	2:20	0
3/29/57	18:09	1:51	1	(1) Belt on air conditioner broke	:00	2:24	0
TOTALS	410:43	9:17	23			49:21	3

Reports and Seminars

Seminars

"The Design of Speed-Independent Circuits I. The Basic Approach to the Problem", by James H. Shelly, March 5, 1957.

"Calculation of Fourier Transforms on the Illiac", by Professor Bruce L. Hicks, Control Systems Laboratory, March 12, 1957.

"Symbolic Address Decimal Order Input Routine", by Roger H. Farrell, March 19, 1957.

Reports

Digital Computer Laboratory Report No. 78, "Theory of Asynchronous Circuits II", by D. E. Muller and W. Scott Bartky, March 13, 1957.

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The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, D. B. Gillies, J. E. Robertson, J. P. Nash, A. H. Taub, and R. E. Meagher.

UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

April, 1957

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Design of Arithmetic Unit

The investigation of the use of one's complement representation for negative numbers in an arithmetic unit employing separate carry or borrow storage has been completed. It was found that multiplication requires that the sign of the original contents of the accumulator and carry registers must agree with the sign of the final product, otherwise a complex correction of the least significant part of the final product is necessary. This correction could not be achieved if the adder were a single-length adder. The correction can be accomplished without benefit of extra facilities if at each step of the multiplication the digit which is about to be shifted into the multiplier-quotient register is corrected, which involves the addition or subtraction, depending on the sign of the partial product, of one in the least significant stage of the accumulator-carry register combination. Thus for the cases where the multiplier digits indicate that the multiplicand is added to (or subtracted from) the partial product, the sign digit of the partial product has to be determined by a carry-assimilation to the sign-digit, and depending on the sign either an addition or a subtraction of one has to be performed before the least significant digit of the accumulator-carry register combination can be shifted into the multiplier-quotient register. Since assimilation is required for each addition or subtraction, the one's complement multiplication will be slower than the corresponding two's complement multiplication. Although the one's complement scheme is useful in a division process which yields a truncated quotient and a corresponding remainder, the complexity of the multiplication is felt to offset that advantage. We conclude therefore that the one's complement scheme is not practical for an arithmetic unit with separate carry or borrow storage.

2. Memories

Word Arrangement Memory

The transmission line delay effect of signals traveling through the magnetic switches was investigated. With the particular configuration of windings through the switch used in the one word test memory, the delay was found to be approximately 2.3 mμs per switch. For a matrix of 32 x 32 switches, a maximum delay of 75 mμs should be expected. The characteristic resistance of such a line is around 200 ohms. This value, however, is subject to further changes.

Details of this test and results will be included in the later report on core memory.

Some investigation regarding the uniformity of cores have been carried out to determine the feasibility of non-destructive readout core memory. Any useful results in this aspect would also be included in the report on core memory.

Fast Readout for Word Arrangement Memory

There is a possibility that the word-arrangement memory with partial switching, as described in the progress report for March could be modified to provide very fast non-destructive sensing. If this possibility can be realized, which is by no means certain as yet, an auxiliary very high-speed memory might not be necessary.

This possibility of non-destructive sensing results from the fact that one of the cores representing a given bit is only partially magnetized (or even practically demagnetized) whereas the other is completely magnetized. The slope of reversible magnetization curves for cores in these two states differ considerably. If the slope of the flux-current curve for the saturated core is represented by L henries and that of the partially magnetized core by L' henries, the output voltage of the pair when a current pulse passes through the cores is $\pm(L'-L)\frac{di}{dt}$, where the sign of the output depends on whether a "0" or a "1" was stored. Provided the pulse is less than .4 amperes no permanent change in the state of the cores would occur. The magnitude of the output voltage from such a pair of cores would be of the order of 10 or 20 millivolts. The ratio of L' to L is nearly 2:1 and for the few cores so far tested the maximum deviation in L' or L from core to core does not exceed ±5%. Previous methods of non-destructive

sensing have been based on the curvature of the hysterisis curve at the remanent point which provides a smaller and less consistent output signal.

One difficulty regarding the application of the idea of non-destructive sensing described above is that it is very doubtful whether the small fast pulses required could be handled by the switch-core array. It would be likely that a separate selection device would be needed for these pulses. Provided that the currents were small enough a diode matrix might be used for this purpose.

The time required for writing information into the memory would not be affected by this suggestion for reading.

Fast Diode Capacitor Memory

The problem of large current drives for a fast access diode capacitor memory has not been resolved.

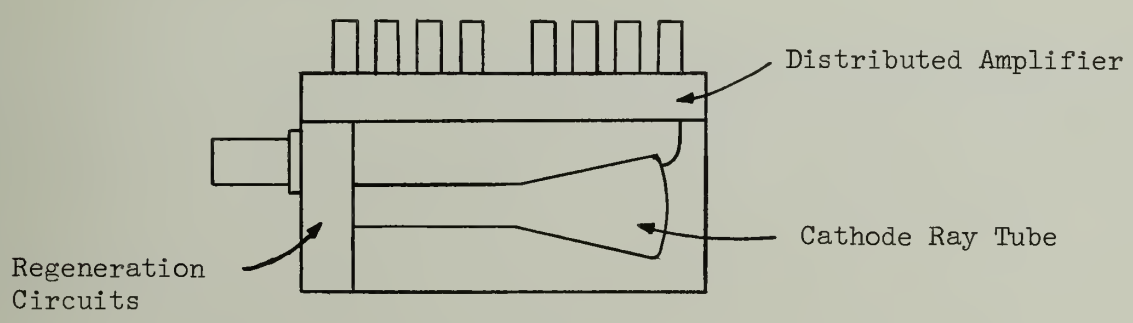
The low back resistance of available fast recovery diodes necessitates large values of storage capacitance in order to provide sufficiently long storage times. Driving capacities of this order in a fraction of 100 mμs requires pulses in the ampere range. This situation will likely hold until higher back resistance fast diodes can be found.

A report on this is being written but no additional work is contemplated.

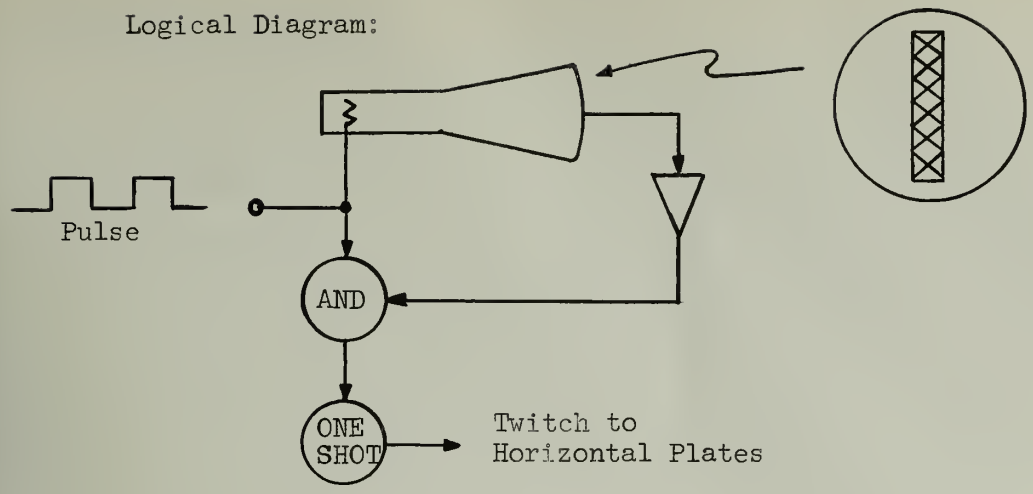
Fast Williams Memory Experiment

An experimental memory has been designed to investigate further the possibility of a memory with 0.1 to 0.2 μs access time. An arrangement has been devised which looks promising for high-speed operation. The storage spots are to be placed in a single vertical row on the tube with the twitch signal on the horizontal plate. Only one pulse is required which turns on the beam and gates an AND circuit. Then depending on the polarity of the resulting signal, the beam may or may not be twitched for the remaining time of the pulse.

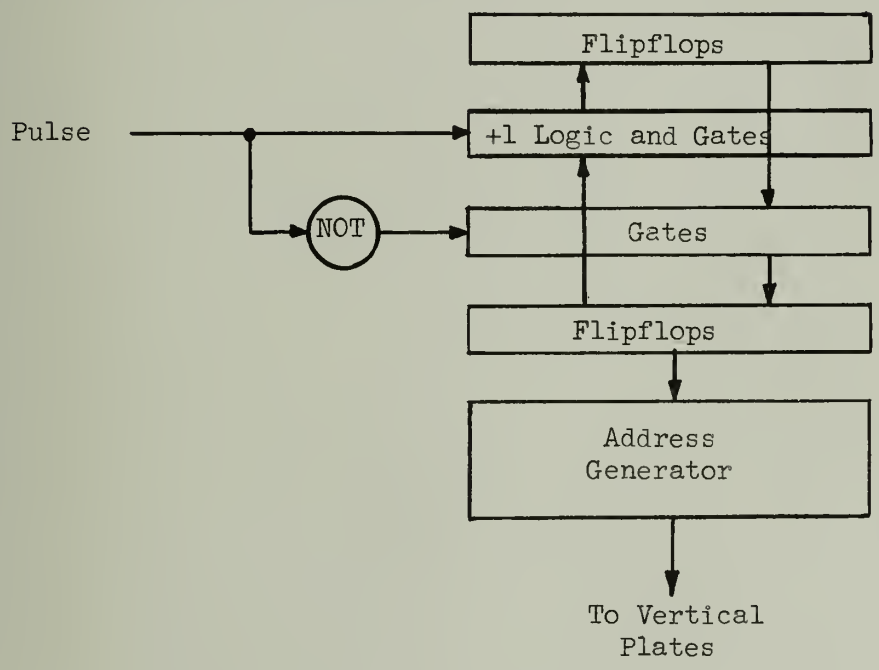
Physical Arrangement:



Logical Diagram:



The address counter could be of the dispatch type as is used in Illiac and would be arranged as shown below:



Sufficient equipment is under construction to test the fast memory system at a single address. The distributed amplifier and circuit mount are nearly finished. Considerable attention has been paid to the problems of shielding and lead length.

3. High-Speed Circuits

The program of designing a new set of logical elements using Western Electric type GA-53233 transistors has continued. Much of the effort has been devoted to mechanization of the process of calculating flipflops which use two resistor-divider networks to secure last-moving-point signals at the output(s). The design of this type of circuit requires rather extensive calculations, especially if non-linear elements, such as diodes, are used. The mechanization of this calculation, in the form of an Illiac program, has been completed. This program (number 982) is applicable to several varieties of flipflop, NOT circuit and level restorers which are being considered for extensive future use.

Register designs are being considered using the logical elements with ± 2 volt signal levels. A register using a logical arrangement very similar to that of Illiac is being designed and a register with complete speed independence is being designed. A C-element necessary for the latter has been designed.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

One of the problems associated with the design of a speed-independent arithmetic unit is the design of a sufficiently fast shift counter. Although counting may be carried out at the same time as the shifting operation if the execution of a count takes longer than a shift then shifting will be slowed and the counter will limit the shifting speed. A speed-independent design has been achieved, however, in which the counting speed equals the shifting speed, so that in no case will the speed of counting limit the speed of an operation.

This counter contains four seven-bit registers. Initially, the number of shifts is gated into one of these registers from a separate register. The counter then counts downward toward zero, using two of the registers for keeping track of the borrows which occur during the down-counting process in the same way that carrys and borrows are held in the accumulator. The end of counting is sensed by noting that the original seven flipflops have all reached zero. It can be shown that in all cases the borrow registers also contain zero at this time so that no operation equivalent to assimilation is ever required. Thus no steps other than those taking place within the shift time are needed and the counting is achieved without any additional delay.

PART III

MATHEMATICAL METHODS

1. Programming. (Supported by Office of Naval Research under Contract N6ori-07130.)

Tests of the New Eigenvalue Program

The routine using Givens' method for finding eigenvalues of a symmetric matrix has been programmed and a number of tests of it have been made. Special matrices whose roots were known and which had orders 25, 42, 59, 76 and 127 were tested. Results were good to ten decimal places in all cases. The following times were noted.

Order of Matrix	Total Time for Solution
25	7 minutes
42	15 "
59	30 "
76	65 "
127	185 "

Symbolic Address Routine

The programming of the revision of the Symbolic Address Decimal Order Input (called SADOI) has been completed. In this revised version it is not only possible to write arbitrary symbolic addresses, placing them in parentheses, but also to add an arbitrary integer to such an address. This is done by placing the integer after the function digits of the instruction and before the symbolic address.

A comparison postmortem for use with this input routine has also been prepared as well as a routine for printing the list of symbolic addresses opposite their decimal equivalents.

2. Numerical Analysis. (Supported by Office of Naval Research under Contract N6ori-07130.)

Numerical experiments were conducted on the use of the iterative method for solving systems of linear equations described in the March 1957 technical progress report. In these experiments, floating point routines were used. An

examination of the results obtained shows that because of the loss of accuracy inherent in the use of these routines it is difficult to formulate a criterion for termination of the iteration procedure which exploits the full accuracy of the computational sheme. Work is in progress on a program which uses fixed point arithmetic.

3. Hydrodynamic Flows with Shocks. (Supported by National Science Foundation.)

It has been shown* that whether or not a shock is present the conservation equations of hydrodynamics may be written in a form which in the one dimensional case with no external forces acting reduce to

$$\frac{d}{dt} \int_{x}^{x+\Delta x} dx = - (\rho u)_{x+\Delta x} + (\rho u)_x$$

$$\frac{d}{dt} \int_{x}^{x+\Delta x} \rho u dx = - (\rho u^2 + p)_{x+\Delta x} + (\rho u^2 + p)_x$$

$$\frac{d}{dt} \int_{x}^{x+\Delta x} \rho(\frac{u^2}{2} + E)\, dx = - [\, \rho u(\frac{u^2}{2} + E + \frac{p}{\rho})]_{x+\Delta x}$$

$$+ [\, \rho u(\frac{u^2}{2} + E + \frac{p}{\rho})]_x$$

where x and x+Δx represent points in an Eulerian coordinate system, u is the velocity relative to these coordinates, ρ is the density, p is the pressure and E is the specific internal energy.

These equations lead to a variety of difference equations and differential difference equations for the determination of the hydrodynamical variables in terms of their initial and boundary values. Codes based on these equations are being written and numerical experiments are being planned for the comparison of the efficacy of the different schemes.

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* A. H. Taub, On the derivation of difference equations for hydrodynamics, Los Alamos Scientific Laboratory Report LA-2073 (1957).

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During April specifications were presented fof 28 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 966. Numbers followed by T are for theses.

966 Computer. Resistor Analysis. The program reads in a list of resistor values and prepares a distribution curve by various methods. It is to be used to determined an appropriate representation for the distribution function.

967 T Physical Education. Attitudes of University of Illinois Students toward Required Physical Education. The general problem is to analyze the results of an attitude survey administered to 1963 women and 3615 men in physical education service courses. The questionnarie, besides reference material, consisted of 10 questions, 5 of which were answered "yes," "no," or "not sure." The other 5 questions were on a 0, 1, 2,..., 8 basis. The significance of difference in response by men and women, and by other divisions of the data, are being determined by Chi square.

968 T Mechanical Engineering. Turbulent Heat Transfer in Liquid Metals. A model has been set up to predict the surface coefficient of heat transfer as well as the temperature profile in a fully-developed pipe flow. Molecular motion and turbulence are both taken into account. The validity of the model will be ascertained by comparing calculations based on it with experimental results. These calculations involve merely a simple integration which will be carried out by Simpson's rule.

969 Physics. Magnetic Field in Rectangular Solenoid. In the experimental investigation of the polarization of n-mesons in cosmic radiation it is necessary to calculate longitudinal components of the magnetic field in a solenoid. This is done using a standard formula.

970 T Electrical Engineering. Properties of Negative Elements in Ladder Networks. By an exhaustive study of various ladder networks an attempt will be made to learn the interrelationships between various component values and the driving point impedances.

971 Mechanical Engineering. Pressure Distribution on Afterbody in Axially Symmetric Supersonic Flows. By use of the code already developed under Problem No. 866, it is intended to calculate the pressure distributions on afterbody of different configurations (e.g. ogive or conical boattail) and the free jet boundary thereafter, in axially supersonic symmetric flow problems.

972 Illinois Water Survey. Estimation of Lake Sediment. An estimation equation is desired which will be used to estimate future sediment collections in reservoirs and lakes. Correlation and regression techniques will be used to determine the efficiency of several variables in determining sediment deposited in 20 Illinois lakes and ponds. The end product of the analysis is an estimation equation for lake sediment deposits based on about 3 of the most efficient variables in the study.

973 T Physics. Angular Distribution of Photo π^+ Mesons from Hydrogen. A least squares fit is to be made of the angular distribution of photo π^+ mesons from hydrogen. The betatron is used to generate 300 mev bremstrallen which bombard a liquid hydrogen target. The experiment is designed to investigate a possible rise in the cross-section at forward angles which is predicted by field theories.

974 Agronomy. Check Data Tapes for K-13 Program. This program will count signs and terminating symbols on data tape prepared for Library Routine K-13. Errors will be noted and printed out.

975 Theoretical and Applied Mechanics. Inelastic Behavior of Aluminum Alloy I-Beams with Elliptic-Type Web Section Cutouts. This program will be used to optimize the design of beams from which the center material has been removed. The variation of beam strength with the shape of the removed section will be studied.

976 T Food Technology. Irradiation of Chickens. Organoleptic and bacteriological data are to be analyzed to determine if Gamma radiation affects organoleptic ratings and if these radiations have a preservative action in terms of microbiological spoilage.

977 T Structural Research. Evaluation of Strain for A Beam-Column. The problem is to determine at any given instant, the extreme fiber strain at two particular sections along the length of A beam-column by use of measured deflections.

978 Psychology. Full Factor Analysis. A study will be made of the validity of partial factor analyses by comparing their results with full factor analyses.

979 T Psychology. The Relationship between Semantic Factors and Recall of Words used in Self-Description. The purpose of this study is to determine what factors, other than the denotative, are related to the recallability of 30 words which are frequently employed in self-descriptions. The recall of these words will also be related to the size of the subject's descrepancy between his rating of the 'real' and 'ideal' self.

980 T Calculation of Temperature Independent Terms for Isotope Effects in Reaction Kinetics. A formula will be used to calculate the temperature independent factor for the isotope effect for various four-body models.

981 Engineering Physics, Navy Pier. Vibration and Rotation Frequencies of Molecules. A consistent set of force constants for closely related molecules will be sought. This will be done by comparing the frequencies computed from assumed sets with observed frequencies.

982 Computer. Symmetrical Flipflop Verification Code. This routine evaluates a large number of algebraic expressions which solve for a number of parameters in terms of given parameters. These solved-for parameters are used to evaluate the performance of a transistor, symmetrical flipflop.

983 T Physical Education. Study of Children's Hearts. The heart size of 75 children will be correlated with age, height, weight, and linear and pulse wave measurements.

984 Sociology. Factors in Community Action Programs. 17 community action programs have been analyzed and 27 variables which enter into the programs have been scaled as to degree of success in the project. The research problem is to find the factors which seem related to success or failure of community action programs and to discover likenesses and differences among the communities involved. It is proposed to seek a principal axes solution to the correlations of the variables, then to rotate to simple structure by the quartimax program. The same procedure will be used for the transform of the correlation matrix to discover factors among the communities. If possible a multiple "r" will be computed to discover the degree to which the estimated success of the programs vary according to the variables. The ultimate goal of this research is to establish a method for describing the causes of failure or success of community action programs. If these causes could be ascertained the effectiveness of such programs might be improved.

985 T Psychology. Meaning System Conflict and Emotional Disturbance in a Multi-Level Personality Theory. The responses of 50 persons on 30 test items selected from the Ewing Personal Rating Form have been collected. To reduce these data to factor scores, several computation steps will be required. These are: 1. Calculation of 30-variable correlation matrix, R. 2. Extraction of factor vectors to get the factor matrix, F. 3. Inversion of R. 4. Forming the triple product, $M R^{-1} F = P$, where P is the matrix of factor scores, and M is the matrix of responses on the Ewing Test. Prior investigation has resulted in factor scores for the same 50 subjects on three other psychological tests. These three tests together with the Ewing Personal Form operationally represent four levels of consciousness. The psychological hypothesis to be tested is that the greater the discrepancy among a person's factor scores over these four tests, the greater will be the degree of emotional disturbance. This discrepancy will be measured by subtracting each factor score matrix from each of the others. Finally a multiple correlation coefficient will be calculated using the factor scores on all of these tests as predictors with psychotherapists' ratings as a criterion.

986 T Physical Chemistry. Calculation of Normal Frequencies in C^{13} Substituted Formic Acid. Using data on the normal frequencies of C^{12} formic acid one may compute the molecular force constants. If the C^{13} mass is then substituted for the C^{12} mass one may then compute the frequencies for C^{13} formic acid.

987 T Agricultural Economics. An Analysis of Wholesale and Retail Prices of Selected Processed Feeds. Simple correlations will be calculated between one retail price and three previous wholesale prices of five selected feeds in Illinois. The purpose of the investigation is to determine the wholesale price most nearly associated with a given retail price.

988 Agricultural Economics. Hog Carcass Evaluation. This program will relate various carcass characteristics with yields of wholesale cuts of pork.

989 Computer. Integration of Partial Differential Equations. An investigation will be made of various methods for integrating hyperbolic partial differential equations.

990 T Psychology. Motivation Factors. This is a study of factors in human motivation. A variety of manifestations of interest - attention, memory, physiological signs, etc., are being factored to test the psychoanalytic hypothesis that three contributers - ego, id, and super ego - will be found involved in any typical interest.

991 T Electrical Engineering. Influence of Electron Interaction on Resonance Width. Effects of electron interaction on the broadening of cyclotron resonance in a gaseous discharge plasma will be studied. Two simultaneous ordinary differential equations which describe the rate of change of the electron velocity distribution function will be solved using standard methods.

992 Agricultural Economics. Change in Community Habits Following the Occupation of Japan. The purpose of this research is to study changes in rural communities in Japan: family, social, organizational, land ownership, etc., as related to a similar study made in 1947.

993 Agricultural Economics. Participation of Rural Illinois People in Social Organizations. Comparisons will be made with the results of a similar study made in 1933, to determine changes in the extent to which farm people in Illinois participate in social organizations.

Table I shows distribution of machine time for the month of April.

TABLE I

	Hrs:Min.
Regular Maintenance	39:11
Unscheduled Maintenance	6:21
Drum Engineering	38:40
R.A.R.	5:51
Leapfrog	41:18
Wasted	
Use by Departments	
Computer Group	43:28
Physics	24:03
Control Systems Lab.	63:52
Structural Research	52:11
Struct. Res. (AF 24994)	14:21
Theor. and Appl. Mech. (Task 53)	4:15
Theor. and Appl. Mech. (1834 (14))	2:25
Psychology	35:24
Elec. Eng. (AF 1406)	1:43
Elec. Eng. (Nobsr 64723)	14:03
Elec. Eng. (A T 392)	:14
Electrical Engineering	11:59
Elec. Eng. (AF 28634)	:04
Chemistry	61:16
Agriculture	23:40
Illinois Public Welfare	:13
Quartermaster Food Institute	:26
Mech. Eng. (AF 18 392)	2:23
A.F. 3203 Redwing	:32
Classes	23:32
Demonstrations	1:41
Miscellaneous	35:22
	548:28

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for April.

TABLE III

Reader Errors	3
Punch Errors	1
Control Errors	1
Power Supply Errors	1
Drum Errors	11
Unknown Errors	1
Total	18

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
4/1/57	20:00	:00	0		:00	4:34	0
4/2/57	20:00	:00	0		:00	2:00	0
4/3/57	20:00	:00	0		:00	:54	0
4/4/57	20:00	:00	0		:00	:40	0
4/5/57	20:00	:00	0		:00	2:06	0
4/8/57	20:00	:00	0.		:00	:47	0
4/9/57	18:38	1:22	2	(1) Reader "J" Error (2) Reader "J" Error	:00	1:13	0
4/10/57	20:00	:00	0		:00	1:13	0
4/11/57	20:00	:00	0		:00	:41	0
4/12/57	19:55	:05	1	(1) Punch #3 Error	:00	:45	0
4/15/57	19:59	:01	1	(1) Reader "F" Error	:00	:45	0
4/16/57	20:00	:00	0		:00	:42	0
4/17/57	17:38	2:22	2	(1) Control Error (2) Unknown	:00	:55	0
4/18/57	19:31	:30	1	(1) Drum Error	:00	:58	0
4/19/57	19:44	:16	2	(1) Drum Error (2) Drum Error	:00	:49	0
4/22/57	19:31	:29	3	(1) Illiac Power Supply Failure (2) Drum Failure (3) Drum Failure	:00	1:02	0
4/23/57	19:59	:01	1	(1) Drum Failure	:00	1:03	0
4/24/57	19:59	:01	1	(1) Drum Failure	:00	1:20	0
4/25/57	19:59	:01	1	(1) Drum Failure	:00	:40	0
4/26/57	18:26	1:34	1	(1) Drum Failure	:00	:40	0

TABLE II Continued

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
4/29/57	19:22	:38	1	(1) Drum Failure	:00	:53	0
4/30/57	19:59	:01	1	(1) Drum Failure	:00	:49	0
TOTALS	432:39	7:21	18		:00	25:29	0

Reports and Seminars

Seminars

"One Possible Logical Arrangement for the New Computer", by Professor Donald B. Gillies, April 2, 1957.

"Eigenvalues in Modern Industry: Problems Involving Differential Operators", by Dr. David M. Young, Ramo-Wooldridge Corporation, April 8, 1957.

"Eigenvalues in Modern In Modern Industry", by Mr. Werner L. Frank, Ramo-Wooldridge Corporation, April 23, 1957.

"Small Capacity Fast Access Memories", by K. C. Smith and G. H. Leichner, April 30, 1957.

Personnel

The personnel associated with the group and hence the contributors to this report are:

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Farrell, Roger H., 1/2 time Research Assistant
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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are

not, in general, reported herein.

Part I: Study Program on High-Speed Computer

Part II: Switching Circuit Theory

Part III: Mathematical Methods

Part IV: Illiac Use and Operation -
General Laboratory Information

May, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Design of Arithmetic Unit

Additional reasons for the choice of the two's complement representation of negative numbers were found. During multiplication, a partial product is represented as n digits in the accumulator A plus k digits of the final product in the quotient register Q. If an n digit addition or subtraction is performed such that the new contents of the accumulator differ in sign from the original contents, then the n+k digits correctly represent the sum or difference only if the two's complement representation is chosen. In particular if, as in multiplication, the addition or subtraction is followed by a right shift, either the k digits in the quotient register must be changed, or the least significant digit of A must be corrected before insertion into Q, for one's complement or absolute value representations.

Thus, either an unrestricted hold multiply, or a multiplication method with multiplier digits recoded as -1, 0, or +1, is more difficult to mechanize if a negative number representation other than two's complement is chosen.

2. Arrangement and Control

Because of the expense of 4-word transfers between the fast memory and the core memory, and because a word length of more than 40 bits is under consideration, so arithmetic may be slower, design studies were made for a computer using 2-word transfers only. Such a machine can be made virtually as fast as a 4-word transfer machine except for problems having few multiplications or divisions. Among the features under consideration for such a machine are the following:

a. Data and instruction transfers take place between the fast memory and the core memory during arithmetic.

b. Future instructions are read from the fast memory, their addresses modified or the counting performed, and an operand is read into a buffer register between the fast memory and the arithmetic unit, during arithmetic.

c. Block transfers of variable length may be performed between the two memories, automatically or under program control.

d. The fast memory may be divided in several ways into regions for instructions and data, and the B-registers may be used with either as counters or modifiers.

e. Transfers between drum, tapes, input-output equipment, and the core store are done during any of the above operations.

The problem of retaining as much accuracy as possible in floating point is being considered. The accumulation of sums of products to higher precision appears feasible using the same equipment as "add product" and floating point addition. No way has yet been found to facilitate double length floating point addition.

The possibility of time-sharing the arithmetic unit with two or more memories is also being considered as a possible machine organization system.

3. Memories

Report No. 79 has been prepared on the one-word arrangement memory. Further work on this memory is anticipated on (1) the test of a plane of 64 x 64 cores and (2) a more thorough experimental test of the non-destructive readout system discussed in Report No. 79 and in the April progress report.

The equipment for an experimental test of a fast Williams memory has been built and is about ready to be tested. As reported earlier, the equipment will make possible the test of a 0.1 μs access period Williams memory.

4. High-speed Circuits

A set of 4 flipflops, a NOT circuit, an AND circuit, and an OR circuit have been designed using the diffused-base transistors and $\pm$2v as the signal levels for the binary digits. These circuits will make it possible for informa-

tion to go through three stages of logic before operating another flipflop or about six stages of logic before going through a NOT circuit. This is a considerable improvement over previous circuits in which a ±1v signal was used to represent the binary digits. These circuits use diodes to keep the transistors out of saturation. The circuits are being incorporated in an over-all report on the study program.

5. Report on Study Program

A report is being prepared which summarizes the year's work on a high-speed computer and outlines its design. This report is partly in draft form. It will have the following chapter headings:

I. Problems Requiring Faster Computers

II. Requirements on a Very Fast Computer

III. Proposed Machine (General)

IV. Basic Circuits

V. Asynchronous Circuits

VI. Memory Hierarchy

VII. Input-Output

VIII. Arithmetic Unit

IX. Registers

X. Control

XI. Sample Problems

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

Further results have been obtained in the theory of distributive circuits which are pertinent to the general synthesis procedure described in earlier reports.

The partially ordered set of C-signals must satisfy several conditions if it is to describe a distributive circuit. Those conditions which are necessary and sufficient for the set of C-signals to give rise to a distributive lattice of numerical vectors have been mentioned earlier. The remaining conditions result from the requirement that the circuit be realizable in terms of logical elements (hardware) which behave in a consistent fashion and which are capable of producing but a finite set of signal levels. Two of these remaining conditions have been found.

a. The first condition is that the partially ordered set of C-signals should be either finite or else be decomposable into a finite part and one or more infinite parts which exhibit cyclic structure. Each of the cyclic infinite parts consists of a basic cell which is repeated infinitely after its first occurrence.

b. The second condition pertains to the structure of these infinite parts. If two C-signals (α,i) and (B,j) within such an infinite part bear the ordering relation $(\alpha,i) \leq (B,j)$, then there must exist a C-signal (γ,i) having the property that $(B,j) \leq (\gamma,i)$.

It is thought that these two conditions, together with the earlier ones, are not only necessary but also sufficient for realization of the circuit provided one introduces additional nodes in some cases. If this is the case, the synthesis problem will be reduced to determining ways to introduce these additional nodes. Future work will be concerned with proving the sufficiency of these conditions and the development of techniques for introducing additional nodes which make the circuit realizable.

PART III

MATHEMATICAL METHODS

1. Numerical Analysis. (Supported by Office of Naval Research under Contract N6ori-07130.)

Numerical experiments on iterative solutions of linear equations continued. It was learned that if the calculations are made using fixed point arithmetic operations and if the residual vector was computed in double precision more accurate solutions were obtained than if floating point arithmetic was used.

2. Flows Behind Shocks. (Supported by National Science Foundation under Grant G-2794.)

The program for the computation of stationary or pseudo-stationary flow behind a given shock has been completed and checked out. The code in its present form can deal with up to 50 evenly spaced points on the initial curve (shock). The restriction to 50 points is due to the fact that only the Williams store is used; the program can be easily altered to accommodate more points by making use of the magnetic drum. The input data consists of an indication of whether the flow is stationary or pseudo-stationary, the number of points on the shock, n,

c_1 = speed of sound in the region ahead of the shock (constant),

$\alpha(i\ s,0)$ = inclination of the shock for $i = 0, \ldots, n-1$,

$\theta_1(0,0)$ = inclination of the (uniform) on-coming flow,

$m_1(0,0)$ = Mach number of the (uniform) on-coming flow,

γ = ratio of specific heats of the gas being treated,

Δs = interval between points on the shock,

ε_{min},

where $\varepsilon_{min} > 0$ is the smallest value of $\varepsilon = \lambda\,(1-m^2\sin^2(\theta-\alpha))$ which will be tolerated during the computation (the boundary of the region of regularity of the flow equations is composed of points for which $\varepsilon = 0$).

The computation proceeds by first solving the Rankine-Hugoniot equations to obtain the initial values immediately behind the shock and then by integrating the flow equations behind the shock in the form given by Taub (Am. Math., 62, pp 300-325) by means of a first order difference scheme. The output consists of the quantities

$$\xi_1(s,T) = \frac{1}{\gamma} \log \frac{p(s,T)}{p_1(s,T)} \qquad (p = \text{pressure})$$

$$\theta(s,T) = \text{inclination of the flow behind the shock}$$

$$c(s,T) = \text{speed of sound behind the shock}$$

$$m(s,T) = \text{Mach number behind the shock}$$

$$\lambda(s,T) = \text{length of tangent vector to displaced shock}$$

$$\alpha(s,T) = \text{inclination of the displaced shock}$$

$$\mathcal{E}(s,T) = \lambda(1-m^2\sin^2(\theta-\alpha))$$

at all points (s,T) such that $s = i\Delta s$, $T_j = \sum_{k=1}^{j} \Delta_k T$, where $0 \leq i + j \leq n - 1$ and

$$\Delta_1 T = \frac{\Delta s}{2} \min_{0 \leq r \leq n-1} \mathcal{E}(r\Delta s, 0); \quad \Delta_k T = \frac{\Delta s}{2} \min_{0 \leq r \leq n-k} \mathcal{E}(r\Delta s, T_{k-1}).$$

The $\Delta_k T$, which are chosen to satisfy the stability condition for the difference equation, are included in the output.

A number of cases of straight shocks in both stationary and pseudo-stationary flow have been tried on the machine with satisfactory results.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During May specifications were presented for 18 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 994. Numbers followed by T are for theses.

994 Economics. Rate of Growth. The problem is to determine a function of one variable from a non-linear difference equation of varying order, representing the proportionate equilibrium rate of growth of gross national output in a 2-region economical model. The method used is recursive algebraic, using floating point arithmetic.

995 University of Sydney (Australia). Earth Dam Stability Determination. The program carries out earth dam stability determinations by the trial slip circle method. About half the program consists of comparison of relative magnitudes of numbers leading to selection of appropriate numbers. The other half consists of some very simple calculation and some interpolation. The output from one trial is a single number which is the safety factor for sliding failure along the chosen circle arc and under the chosen conditions. This program will only be checked on the Illiac and is for use with the Silliac.

996 Economics. Stability of Economic Growth. A simple system of difference equations illustrating the structure of the United States economy has been constructed. A solution of this system should reveal (1) the long-run proportionate rate of growth in equilibrium, (2) the tendency or lack of tendency of the system to return to its equilibrium path if disturbed.

997T Chemistry. Spectrum of General 4-Nuclei Spin $\frac{1}{2}$ System. The problem is to calculate the spectrum of transition energies and their intensities for a general system of four interacting nuclei of spin $\frac{1}{2}$, each of which sees a slightly

different external magnetic field. The interaction energy is of the same order of magnitude as the difference in energies due to the different external fields. This general system can be particularized to several simple cases (e.g., 3 interaction spins, cases where two or more nuclei see the same external field.).

998T Chemical Engineering. Turbulence Levels. Turbulence levels are being measured with a hot-wire anemometer. Calculation of turbulence levels from hot-wire data involves the calculation of coefficients of three linear simultaneous equations, and the solution of these equations for the three unknowns.

999 Computer. Translation of Chemical French. A new system of mechanical translation is being tested. Rules for translation are obtained from a study of actual literature. These rules are codified for use by the computer.

1000 Computer. Correct or Modify R1. The square root routine in the library is to be modified so that it will not stop when presented with the number $1-2^{-39}$.

1001T Psychology. Components of a D^2 Statistic. In studies of interpersonal preception, raters are asked to describe their co-workers on profile questionnaires. The D^2 statistic has been used to evaluate the way a rater preceives his co-workers. The question has come up as to whether the D^2 measure is appropriate for this situation, so old data is being reanalysed, using the correlation coefficient, profile means and profile variances in place of the D^2. In this way an attempt will be made to discover whether any of these scores will predict an outside criterion better than the D^2 does.

1002T Civil Engineering. Response of Spring Mounted Flexural Beam Subjected to Moving Distributed Load. The problem is to determine the effect of relative spring stiffness, yield displacements, magnitude and velocity of loading on the dynamic response of a spring mounted flexural beam. The method of solution involves Newmark's β method and numerical integration methods.

1003 Bureau of Educational Research. Re-evaluation of Criterion Instruments Used to Develop Means of Measuring Teacher Effectiveness. Two instruments used to collect children's opinions of their teachers were administered to approximately 3700 children (138 classes). The two instruments were designed to measure different aspects of the teaching situation, but a correlation of these instruments yielded a Pearson r of .85. This raises several questions. (1) Are the two instruments measuring essentially the same thing? (2) Is there only one general factor involved or are there several relatively independent factors that are being tapped by these instruments? (3) If there are factors other than one general factor involved, are these factors sufficiently weighty to be used as criterion measures? The answers to these questions will come from the production of a 96 x 96 item correlation matrix followed by a centroid factor analysis.

1004T Civil Engineering. Determination of Velocities and Acceleration from Measured Deflections. In the analysis of the results of tests made on beams subjected to rapid loadings, the approximation is made that the specimen behaves as a single degree of freedom system, with the mass of the specimen being replaced by an appropriate value for the effective mass of the substitute system. Values of deflection at the center of the specimen have been tabulated at 1/2 millisecond intervals, from which, by a numerical differentiation procedure, velocities and acceleration may be calculated. The accelerations thus obtained may be used in determining the actual resistance of the beam by assuming that the inertia force is equal to the assumed effective mass multiplied by the acceleration at any time interval.

1005 School of Medicine, Northwestern University. The Ward Milieu: I Value Attitudes of Patients and Personnel. By means of the Q-sort methodology an attempt will be made to identify the nature of the attitude value systems operant in a neuropsychiatric treatment ward. The attitudes of patients, aides, nurses, doctors, and other personnel provide a background which dynamically interacts with the treatment program. Hence, we are seeking a rapid, effective method to identify these attitude value systems and to assess these effects on the treatment program. An 80 item Q-sort was developed consisting of 80 statements reflecting noted attitudes observed in group therapy, interviews and projective testing. Forty-six individuals comprising the total population of the ward were given this attitude scale.

1006 Electrical Engineering. Filter Transfer Loss. Filter transfer loss will be calculated from a formula and tabulated.

1007 Physics. Integration for Quenching Experiments. These calculations relate to experiments on the quenching of gold wires, and will be used to study the role which point imperfections play in diffusion and electrical conduction. The calculation itself involves the integration of ordinary differential equations.

1008 Geological Survey. Mixed-layer Effects in the Rhombohedral Carbonates. Methods which were previously used to study X-Ray diffraction in crystals made up of two kinds of ionic layers which occurred in varying proportions and sequences are to be extended to the three-layer case.

1009T Psychology. Relationship Between Changes in Sociometric Status and Certain Personality Characteristics. Sixteen subtest scores on each of 50 subjects have been obtained. D^2 will be used to measure the difference between the profile of one individual and that of another individual. This measure is needed for all possible combinations of the 50 subjects.

1010 Electrical Engineering. Normal Modes of a Ridged Rectangular Waveguide. This program will use a rectangular mesh over the cross section of a cylindrical waveguide. It will be sufficiently versatile to permit the use of any cross sectional shape, although initially a ridged rectangle will be used.

1011T College of Education. Changes in Student Teachers Through Use of Pupil Ratings. Statistical studies will be made of the change in the pupil ratings of teachers during the teaching period.

Table I shows distribution of machine time for the month of May.

TABLE I

	Hrs:Min.
Regular Maintenance	34:22
Unscheduled Maintenance	14:02
Drum Engineering	49:04
R.A.R.	5:30
Leapfrog	68:19
Wasted	:00
Use by Departments	
Computer	38:18
Physics	39:44
Control Systems Lab.	49:16
Structural Research	41:55
Struct. Res. (AF 24994)	7:53
Struct. Res. (AF 3203)	:19
Theor. and Appl. Mech. (NR 1834 (14))	4:22
Theor. and Appl. Mech. (AF 2753)	1:29
Psychology (M D 569)	:16
Psychology	28:25
Electrical Engineering	23:46
Elec. Eng. (Nobsr 64723)	2:17
Elec. Eng. (AF 33(038)28634)	:31
Elec. Eng. (AF 30(635)1406)	:28
Chemistry	34:01
Agriculture	24:33
Mech. Eng. (AF 18(600)392)	1:50
Quartermaster Corps	2:19
Illinois Public Welfare	3:06
Classes	18:28
Demonstrations	5:32
Miscellaneous	42:23
	542:28

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for May.

TABLE III

Unknown Error	1
Control Errors	4
Memory Error	1
Drum Failures	14
Scope Error	1
Total	21

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
5/1/57	19:54	:06	2	(1) White switch trouble (2) Drum failure	:00	1:36	0
5/2/57	20:00	:00	0		:00	:41	0
5/3/57	19:58	:02	2	(1) Unknown error (2) Drum failure	:00	2:07	0
5/6/57	19:50	:10	1	(1) Drum failure	:00	2:38	0
5/7/57	19:59	:01	1	(1) Drum failure	:00	:41	0
5/8/57	20:00	:00	0		:00	3:03	0
5/9/57	19:44	:16	3	(1) Scope error (2) Drum failure (3) Drum failure	:00	3:48	0
5/10/57	19:51	:26	1	(1) Drum failure	:00	1:39	0
5/13/57	20:00	:00	0		:00	2:19	0
5/14/57	19:39	:21	1	(1) White switch trouble	:00	3:10	0
5/15/57	17:39	2:21	0	Engineering - Looking for white switch trouble	:00	8:50	0
5/16/57	19:13	:47	1	(1) Control error. C-43 filaments turned out.	:00	:40	0
5/17/57	20:00	:00	0		:00	1:22	0
5/20/57	20:00	:00	0		:00	4:38	0
5/21/57	19:38	:22	2	(1) Drum failure (2) Drum failure	:00	5:59	0
5/22/57	18:15	1:45	1	(1) Memory failure position 24	:00	5:58	0
5/23/57	19:46	:14	1	(1) Drum failure	:00	2:21	0
5/24/57	20:00	:00	0		:00	2:49	0

TABLE II (continued)

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
5/27/57	14:53	5:07	3	(1) Drum failure (2) Drum failure (3) Drum Illiac control error - odd order gate chassis had unsoldered drum address lead coming from pin 2 of the 2C51	:00	:51	0
5/28/57	20:00	:00	0		:00	:42	0
5/29/57	18:44	1:16	1	(1) Drum failure	:00	5:18	0
5/31/57	19:55	:05	1	(1) Drum failure	:00	:40	0
TOTALS	426:41	13:19	21		:00	61:50	0

Reports and Seminars

Seminars

"Automatic Programming in Scientific Computing", by Professor J. N. P. Hume, University of Toronto, May 7, 1957.

"The Mechanical Translation of French Chemical Literature", by Professor A. F. R. Brown, Georgetown University, May 14, 1957.

"Vacuum Deposited Films as Computer Memory Elements", by Dr. S. M. Rubens, Manager, Physics Dept., Remington Rand Univac, St. Paul, Minnesota, May 21, 1957.

"System Design Features of a New NBS Digital Computer", by Dr. Alan L. Leiner, National Bureau of Standards, May 28, 1957.

Reports

Digital Computer Laboratory Report No. 79, "A One-Word Model of a Word-Arrangement Memory", by H. N. Yu, C. Pottle and R. W. McKay (University of Toronto), May 28, 1957.

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Teaching and graduate research are not, in general, reported herein.

Part I: Study Program on High-Speed Computer

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Part IV: Illiac Use and Operation - General Laboratory Information

June, 1957

PART I

STUDY PROGRAM ON HIGH SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Design of Arithmetic Unit

A method for decreasing the division time has been devised for restoring division and extended for use with the non-restoring method. Initially the divisor y is standardized to lie in the range $\frac{1}{2} \leq y \leq 1$. At each step of the division process, the partial remainders are shifted left whenever possible such that the quantity from which the divisor is subtracted or added is also standardized.

The method has the advantage of decreasing the number of times the adder is employed and at times permits a reduction of the number of gating operations required for division. The method is immediately applicable to restoring division.

For non-restoring division, the conventional method generates a quotient consisting of +1's and -1's with a trivial quotient conversion. The proposed method requires quotient digits of +1, -1, and 0 corresponding respectively to subtraction, addition, and shifting. It can be shown that it is sufficient to store one such quotient digit, and that a conversion to a quotient digit which is either 0 or 1 can always be made on the basis of information available one step later.

2. Arrangement and Control

A design was produced for a computer with one-word transfers between the core memory and a small number of extra registers. The word length is 52 bits. The equipment required for this machine, in addition to the regular memory and arithmetic unit, is:

2	52-bit arithmetic registers	
2	search registers to hold operands	(52 bits each)

1 extra order register (52 bits)

up to 12 B-lines of 13 bits each,

together with some counters and decoding equipment for a second control. The make-up of a 13-bit arithmetic instruction is:

7	function bits	(called F)
4	address bits	(called B)
2	control bits.	(called C)

If B = 0, 1, 2 or 3, the operand comes from A, Q or one of the two extra registers. If B = 4, 5, ..., 15, a main store address is referred to, to be found in B-line 4, 5, ..., 15 respectively. If C = 2 or 3, that address is to be added to the next 13 bits in the word in which the order is found, and if C = 1 or 3, the address in the B-register is then to be increased by one. Most jump instructions require 26 bits, the last 13, possibly B-modified, give the address of the word containing the next instruction to be executed, and C indicates at which of the 4 possible 13 bit groups in the word the instruction begins.

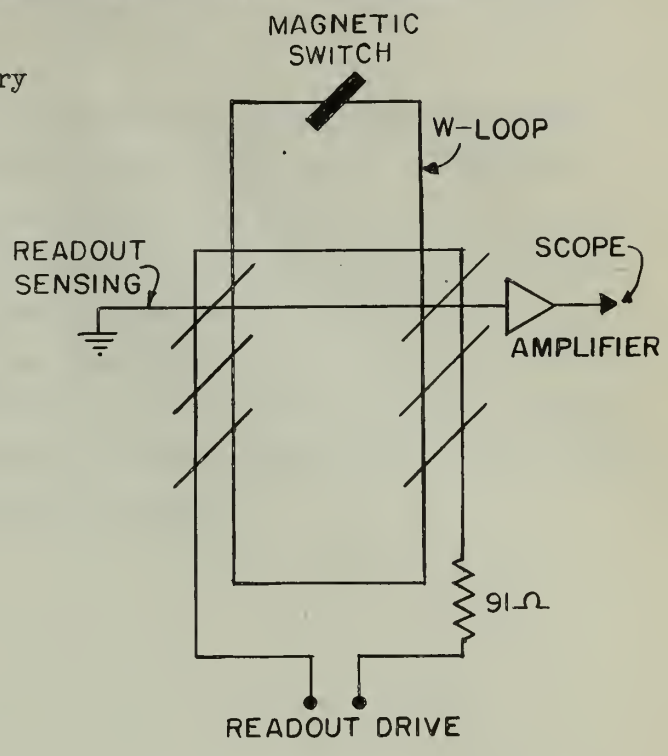
A second control is provided which scans instructions ahead of the normal (arithmetic) control, and reads data between the core store and the two search registers, and from the core store into the extra order register. The two search registers are provided also with addresses so an operand used more than once need not be read out of the core store more than once. Because of the compact order code, the number of references to the main memory for instructions is considerably reduced, and because of the data anticipation system, the main memory is used nearly all of the time.

3. Memories

Non-destructive Readout Core Memory

Some experimental tests are being carried out to determine the feasibility of a fast non-destructive readout core memory. Due to the transmission line delay effect of signals traveling through memory cores, it may not be feasible to adopt such a scheme with a large size memory. However, it appears possible to use non-destructive sensing on a memory of the size of 1024 or 512 words with a random access time of 0.25 μs. approximately.

The experimental readout method on a one-word model is shown in the diagram with all the "writing" wires omitted. Experimental results reveal that the partial switching method of writing into the core memory as discussed in Report 79 is satisfactory and suitable for use in the non-destructive sensing core memory. However, the magnetic switch should be optimized such that maximum output is obtained from the readout. The W-loop which is a closed loop connecting the output of the magnetic switch to the memory core forms essentially a short circuit loop around the memory core. This short circuit loop reduces the output to less than half of that without having this short circuit loop around it. Therefore, it might be necessary to use a current transformer and utilize the W-loop as the readout drive wire as shown in Figure 16 of Report 79.



Future investigations include determining optimum characteristics of the switch core and the current transformer.

Fast Williams Memory

Tests of the experimental arrangement described in the April Progress Report were made. The results indicate that signals are very small, about 1 mv., and that the spot refill process requires 200 mμsec before a detectable change in the read signal occurs. Further tests would require a re-design of the amplifier and are not now contemplated.

4. High Speed Circuits

Tests of engineering samples of fast diodes were continued. No satisfactory replacement for the discontinued National Union diodes (types 37D and 37J) was found.

Characteristics of nine GF 45011 Western Electric transistors were measured and found superior for our switching circuits to the characteristics of the GA 53233.

An effort was made to find suitable drivers to work with transistor gates and flipflops. Both tube circuits and transistor circuits were investigated. The former do not seem suitable because of their low speed and the presence of initial transients.

A transistor driver for 40 bits can be obtained by paralleling two simple drivers, each driving two emitter followers which drive 10 bits each. A suitable fanning procedure using transistors would cost very little in time.

A report (File Report No. 223) which covers the recently completed designs of AND, OR, and NOT circuits for the new computer program was completed during this period. The circuits in question are designed on the basis of the characteristics of some 20 sample GA 53233 transistors and operate with $\pm$ 2 volt signal levels. Several changes are expected to be made in the transistor and diode characteristics which will be reflected in minor modifications of the reported designs.

PART II

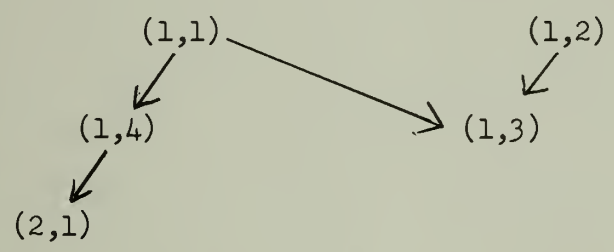
SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. Distributive Circuits

The two conditions given in the previous month's report on the partially ordered set of C-signals were shown to be necessary and sufficient for circuit realization, as was conjectured in May.

The problem of circuit realization, however, appears more complicated than it was originally thought to be. An example was found in which two C-signals, bearing no causation relations to each other, nevertheless, correspond to nodes which are functionally related. The example corresponds to the partially ordered set of the diagram below.



This partially ordered set of C-signals yields a realizable circuit. Its equations are:

$$Z_1' = \bar{Z}_4$$

$$Z_2' = 1$$

$$Z_3' = Z_2(Z_1 \vee Z_4)$$

$$Z_4' = Z_1 \vee Z_4$$

provided the initial state is taken as (0, 0, 0, 0). Here Z_3' is a function of Z_4 in spite of the fact that (1, 3) and (1, 4) do not bear any causation relations to each other in the partially ordered set. Also (2, 1) and (1, 3) bear no causation relations to each other but (1, 1) and (1, 3) do.

In cases such as this, there is no known way of forming the functions without first developing the lattice of C-states. Such a development, though completely systematic, may be very time consuming even though it may be done on the computer. Hence, future work will be directed toward finding ways of avoiding this development.

2. Design of Speed Independent Circuits

The new computer program for testing circuits for speed independence has been revised so that the compiled function routines are made more compact, thus allowing the testing of more complicated circuits. This revised program is being written up for the library.

PART III

MATHEMATICAL METHODS

1. Hydrodynamic Flows with Shocks. (Supported by National Science Foundation)

The program for integrating the one dimensional conservation equation describing hydrodynamical flows with or without shocks given in the April 1957 Technical Progress Report was rewritten so as to allow use of the drum. This was done in order that integrations covering many time steps could be carried out. The results of calculations made with the new code indicate that the density behaves anomalously when the center of gravity of the matter in a fixed Eulerian interval of space is followed in time and used in the interpolation for other dynamical quantities as functions of position.

2. Numerical Analysis. (Supported by Office of Naval Research under Contract N6ori-07130)

A routine for determining the proper values of a symmetric matrix by the method proposed by Givens has been written and placed in the library of subroutines. Methods of determining the proper vectors of such a matrix are under investigation. Since Givens' method reduces the matrix to a tri-diagonal form the determination of the proper vectors involves the solution of the equation

$$B\, y^{(i)} = \lambda^{(i)}\, y^{(i)}$$

with B a symmetric matrix with non-zero elements only along the main diagonal and the two neighboring diagonals. This homogenous set of equations may be solved exactly quite readily. However, obtaining the approximate numerical solution given by a computer involves various difficulties. In particular, since $\lambda^{(i)}$ is not exactly known $\det(B - \lambda^{(i)} I)$ is not exactly zero. Various methods of dealing with the equations for the proper vectors are under investigation including the methods of Wilkinson and Strachey for obtaining the inverses of almost singular matrices.

3. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

M-20 Eigenvalues of a Symmetric Matrix by Givens' Method. This program for finding eigenvalues consists of two parts: rotation to Jacobi form, and use of the Sturm sequence technique to obtain the eigenvalues through binary chopping. During the first part the diagonal elements and one-half of the off-diagonal elements of the matrix being rotated are stored on the drum in such a way that any entire row (or column) may be referred to in a "minimum" access time sequence. Matrices up to order 128 may be handled in this way. During the second part, the entire Jacobi matrix is stored in the high speed memory for greater speed. A check is made on the invariance of the sum of squares of the elements during the calculation. This program is faster and has higher capacity when only the eigenvalues are required than the older library routines which use the Jacobi method.

PART IV

ILLIAC USE AND OPERATION -
GENERAL LABORATORY INFORMATION

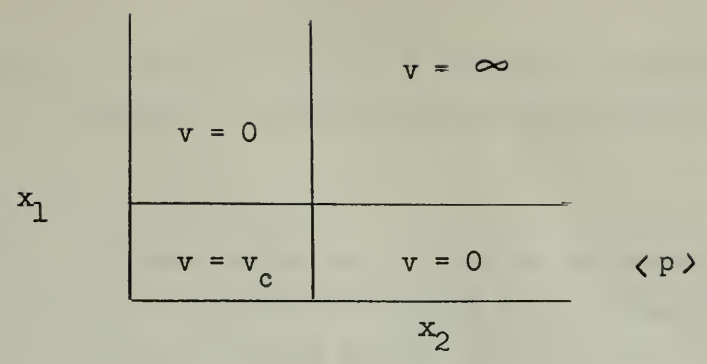
Machine Use

During June specifications were presented for 12 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1012. Numbers followed by T are for theses.

1012 Electrical Engineering. Phase Velocities in Dielectric Loaded Waveguides. The problem consists of the wave propagation constant for partially dielectric loaded rectangular waveguides. The dominant mode is neither TM nor TE, but hybrid and can be used to give a phase velocity in the range of, but less than, the speed of light in free space. It is desired to plot $\frac{\lambda}{a}$ versus $\frac{c}{v}$ for different values of parameters related to the dielectric constant and the geometry of the wave guide.

1013 U. S. Navy. Studies on Career Motivation. This study is an attempt to find out why most enlisted personnel of the Navy near the end of their first enlistment period do not consider the Navy as offering a career opportunity. More specifically the study is designed to increase understanding of the various influences affecting a man at the time of his enlistment and also at various other periods during a subsequent four years. The psychological variables (about 66) will include biographical data, attitudes, knowledge of Navy life, Navy experience, and reenlistment intentions. A group of 6500 recruits will be tested and followed over the period of their Navy career. Selected samples of 600 each will be drawn and tested at 16 periods. Each of these selected samples will be analyzed by calculating phicoefficients, centroid factor analyses, and rotations of factor matrices.

1014 Chemistry. Quantum Mechanical Calculations of Transmission Coefficient in Chemical Reactions. The time dependent Shrodingér equation in two dimensions is to be solved to yield the transmission and reflection of a wave packet by a potential barrier. The geometrical configuration is that shown in the figure.



Preliminary studies of the stability of the numerical method have been made and confirmed theoretically.

1015 Animal Science. Genetic Correlations. The genetic correlation between milk and fat production in cattle will be computed.

1016T Education. Study of Language Ability. Data has been collected on the language ability of two groups of atypical (cerebral palsied) children. Language ability has been indexed by 15 language scores for each child. The cerebral palsied groups are to be compared on these language scores. Mental and chronological age are believed to be important variables affecting language; hence the groups must be equated on these variables before they are compared on the language scores. The problem is to adjust each of the 15 language means for each group to account for differences in mental and chronological age and to then compare the groups on language ability.

1017 Computer Laboratory. Classical Main Sequence Star. The field equations of general relativity describing the spherically symmetric distribution of matter with the equation of state of perfect gas are to be solved.

1018T Civil Engineering. Effect of Roadway Unevenness on Dynamic Response of Highway Bridge. The problem, which is part of the Highway Bridge Impact Investigation, concerns the effect of surface irregularities such as localized obstructions, roughness of deck, and continuous deviation of profile from the assumed smooth horizontal plane on the dynamic response of a simply supported beam.

1019T Industrial Education. Two Experimental Approaches to Teaching Micrometer Concepts and Skills. An evaluation of the relative effectiveness of two teaching methods will be made.

1020 Structural Research. Dynamic Response of Chimneys Subjected to Earthquake Tremors. A vertical cantilever beam is approximated by a system having masses concentrated at panel points. Newmark's Beta method will be used to obtain the dynamic response.

1021 Psychology. Study of Schizophrenic Children. The background characteristics of schizophrenic children will be studied and analyzed statistically.

1022 Physics. Rotation of Coordinates. The problem is to transform the coordinates of points on a photographic plate from one set of rectangular axes to another determined by two reference points on the plate.

1023 Institute of Communications Research. Factorization of "Ways to Live" and Semantic Scales. 13 descriptions of "ways to live" have been rated by 55 subjects on 26 semantic differential scales. Factor analyses of the intercorrelations between the 13 "ways to live" and of the intercorrelations between the 26 scales are to be run using two different procedures for obtaining the intercorrelations.

Table I shows distribution of machine time for the month of June.

TABLE I

	Hrs:Min.
Regular Maintenance	27:20
Unscheduled Maintenance	6:52
Drum Engineering	68:59
R.A.R.	6:18
Leapfrog	61:10
Wasted	:30

Use by Departments

Computer	12:47
Physics	7:57
Control Systems Laboratory	50:17
Structural Research	26:44
Structural Research (AF 24994)	12:49
Structural Research (AF 2303)	:36
Theor. & Appl. Mech. (NR 1834(14))	5:41
Theor. & Appl. Mech. (AF 2753)	1:20
Psychology	26:15
Elect. Eng.	29:47
Elect. Eng. (Nobsr 64723)	2:55
Elect. Eng. (AF 28634)	:27
Elect. Eng. (AF 1408)	1:13
Chemistry	57:27
Agriculture	24:23
U. S. Army Quartermaster Corpe	1:52
U. S. Navy	:17
Ill. Public Welfare Dept. (Hurley)	3:43
Miscellaneous	34:36
Demonstrations	1:31
	477:37

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table

has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for June.

TABLE III

Reader	1
Punch	4
Memory	3
Control	1
Scope	1
Drum Failures	9
TOTAL	19

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/3/57	14:31	2:49	3	(1) Arithmetic Error 2^{-20} * (2) Drum Failure (3) Drum Failure	:00	1:30	0
6/4/57	18:11	1:49	0	Repair time due to drum error previous day			
6/5/57	20:00	:00	0		:00	:50	0
6/6/57	119:59	:01	1	(1) Reader error. Reader K	:00	3:16	0
6/7/57	19:30	:00	0		:30	5:41	0
6/10/57	20:00	:00	0		:00	5:17	0
6/11/57	19:42	:18	2	(1) Drum failure (2) Drum failure	:00	1:06	0
6/12/57	20:00	:00	0		:00	2:56	0
6/13/57	20:00	:00	0		:00	2:08	0
6/14/57	19:06	:54	1	(1) Memory failure Pos. 2^{-25}	:00	8:23	1
6/17/57	20:00	:00	0		:00	2:08	0
6/18/57	20:00	:00	0		:00	1:17	0
6/19/57	19:11	:49	5	(1) Memory failure Pos. 2^{-25} (2) Drum failure (3) Drum failure (4) Drum failure (5) Drum failure	:00	:50	0
6/20/57	17:16	2:44	3	(1) Punch #4 failed to punch 1 hole (2) Control error, shift counter (3) Drum failure	:00	1:51	0
6/21/57	19:16	:44	1	(1) Punch #4 failure to punch clean "1" holes	:00	:42	0
6/24/57	20:00	:00	0		:00	:48	0
6/25/57	19:59	:01	1	(1) Punch #4 not punching "1" holes	:00	1:26	0
6/26/57	19:59	:01	1	(1) Scope Output	:00	1:09	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
6/27/57	19:26	:34	1	(1) Punch #3 had wire broken to B gate	:00	2:24	0
6/28/57	20:00	:00	0		:00	:56	0
				*Computer was in operation only 17:20 on this date.			
TOTALS	386:06	10:44	19		:30	47:22	1

Reports, Seminars and Talks

Seminars

"The Inversion of Nearly Singular Matrices", by C. Strachey, National Research and Development Corporation, London, England, June 17, 1957.

Talks Presented at the Association for Computing Machinery National Meeting, Houston, Texas, June 19 - 21, 1957.

"Illiac Operations", by Dr. D. E. Muller.

"A Study of the Order Types and References to Store in some ILLIAC and FERUT Library", by J. H. Chung, C. C. Gotlieb and D. E. Muller. Presented by C. C. Gotlieb.

"An Illiac Program for Simulating the Behavior of Asynchronous Logical Circuits and Detecting Undesirable Race Conditions", by W. S. Bartky and D. E. Muller. Presented by W. S. Bartky.

"A Binary, Parallel, Asynchronous Arithmetic Unit with Separate Carry or Borrow Storage", by Gernot Metze.

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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

July, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research

The University of Toronto is participating in this work through staff members of its Computation Centre and Department of Physics.

1. Length of Logical Chains

The transistor circuits which are being considered have the property that the flipflop circuits and the NOT circuit restandardize the voltages used to represent logical states. However, for economy of parts, the OR and AND circuits do not restandardize the signal but degrade it both by attenuation and small level changes. After a signal passes serially through some number of OR or AND circuits, it may fail to operate subsequent stages of flipflops or NOT circuits. It is important to know how many serial steps should be permitted before restandardization by a NOT circuit or flipflop is required. A study of Illiac circuits has been made to determine this number of steps (called a chain length) and many are listed in Table I.

TABLE I

Chassis	Chain Length
Recognition Circuit	3,3
Decoding Circuit	1,2,3
Memory Interplay Logic	3,3,4,5
Control for Arithmetic II	2,3,4,5,6,7
Cathode Ray Tube Output Presentation	3,
Input-Output	2,4,5,6,7,9

Only the longer chains were looked for and the short chains are not included in the table. Of the 21 chains listed, only five are greater than a length of five. It seems that a chain of at least five logical circuits should be possible before a restoring circuit is required.

Another important requirement on the basic circuits is that for driving a certain number of other circuits, i.e. branching in logical networks. Branches were also counted in some Illiac circuits, and this is shown in Table II.

TABLE II

Chassis	Number of Branches
Decoding	2, 3, 3, 4, 4
Recognition	3, 4
Memory Interplay Logic	2, 3, 3, 2
Arithmetic Control II	2, 2, 3, 3, 3, 4, 6
Cathode Ray Tube Output Presentation	2, 3, 3
Input-Output	2, 3, 4

Of the 24 branches investigated above, there are 1 >4 branches; 6 >3 branches and 17 >2 branches. Thus 3 branches per basic circuit would be adequate for most purposes.

Actually the real question of how much combined branching and how long a chain should be are interconnected problems. The numbers of a chain length of 5 and possible branching up to 3 do nevertheless give the circuit designer an indication of what is required for logical designs which do not require many extra level-restoring and power-driving circuits.

2. Adder Circuit

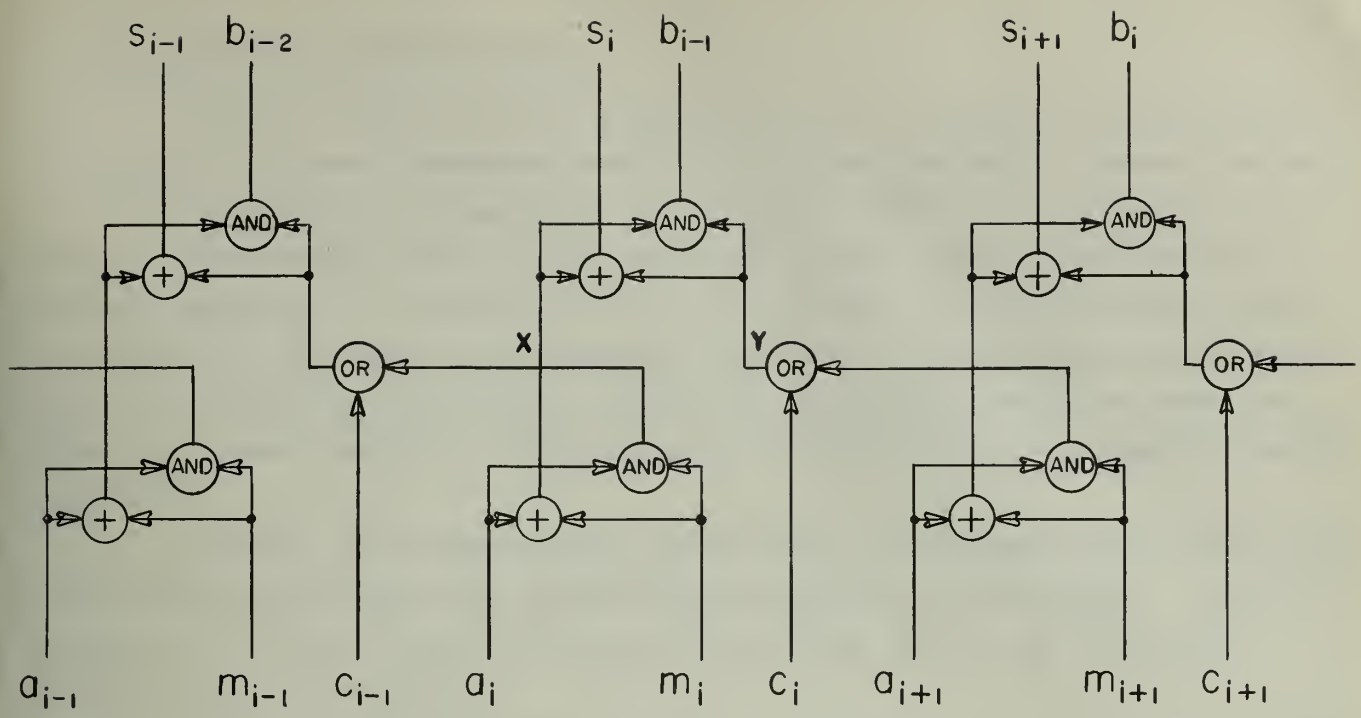
The proposed "adder" structure as shown in Figure 1 was investigated to see where level-restoring circuits, if any, would be required. The basic circuits were considered as those contemplated for the new computer. With a_i, m_i and c_i considered as restored signals, a restoring circuit is required after the OR circuit in each stage, and gating circuits will be needed for both s_i and b_{i-1} which will operate on these signals to set the register ff's. Several ways may eliminate this restoring circuit. They are:

(1) design of a $\oplus$ circuit not requiring restored input signals,

(2) the GF-45011 transistors appear to give smaller deviations in the logical circuits, and may just meet the requirements without restoration,

(3) a combined $\oplus$ and AND circuit with suitable input and output levels may be possible,

(4) some other structure for the adder might be better.



$$s_i = a_i \oplus m_i \oplus \left[a_{i+1}\, m_{i+1} \vee c_i\right] \qquad b_{i-1} = \left[a_i \oplus m_i\right] \cdot \left[a_i + m_{i+1} \vee c_i\right]$$

Figure 1. Proposed Adder Structure

Another adder structure could be as follows:

$$s_i = (a_i \vee m_i)(\bar{a}_i \vee \bar{m}_i) \oplus \overline{(\bar{a}_{i+1} \vee \bar{m}_{i+1})\bar{c}_i}$$

$$b_{i-1} = (a_i \vee m_i)(\bar{a}_i \vee \bar{m}_i)\left[\overline{(\bar{a}_{i+1} \vee \bar{m}_{i+1})\bar{c}_i}\right]$$

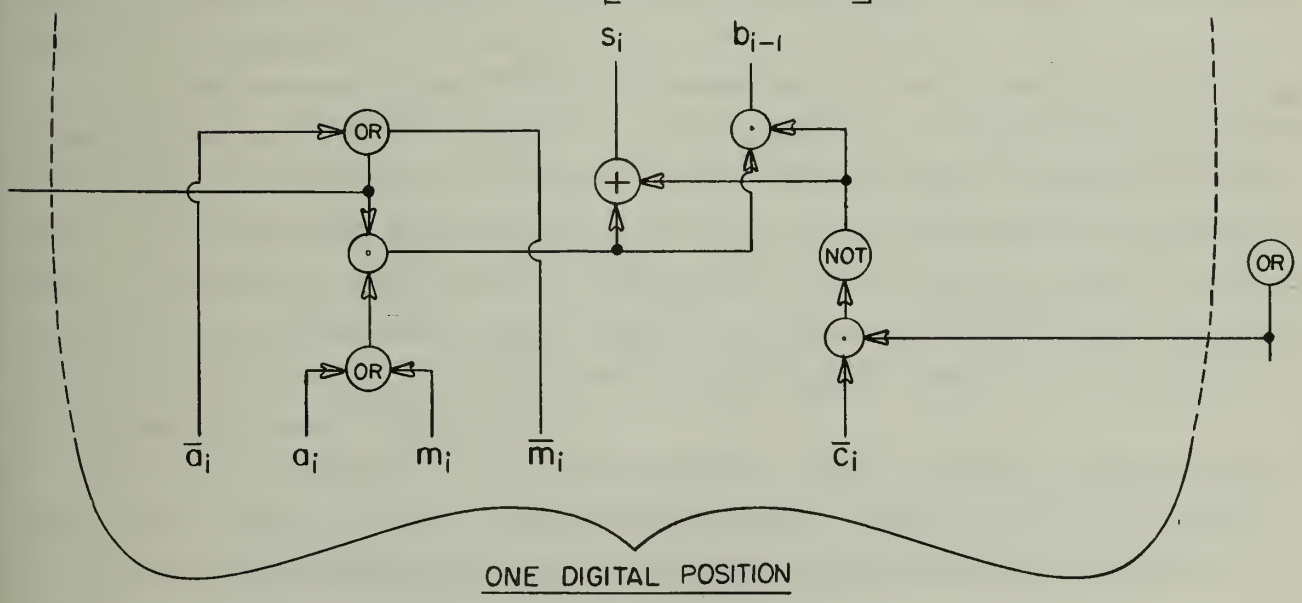


Figure 2. Alternative Adder Structure

3. Non-Destructive Memory Readout

Further experiments have been carried out to determine the feasibility of modifying the word arrangement memory for fast non-destructive readout systems.

It appears that one of the most serious problems in considering such a memory would be that of noise since the output signals from a non-destructive readout system are of the order of 2 to 3 mv. Signal to noise ratio may be improved by using multiple readout turns on cores and by twisting the readout wires. The labor involved in constructing such a memory core plane might be excessive. These requirements prohibit consideration of a large-scale non-destructive readout core memory.

However, a non-destructive sensing memory of the order of 256 words might be a compormise for the noise problem and the problem of construction. The cost per word in this case could be as much as four times that of the destructive readout memory of 4096 words.

Various technical problems will be taken up as soon as a memory core plane of 16 or 32 words may be obtained. Arrangements of slow and fast readout core memories will also be studied.

4. High-Speed Circuits

A set of 18 more GF-45011 transistors has been received from Western Electric, and their parameters have been measured and tabulated. A set of typical transistor parameters has been decided upon in light of the parameters for the above 18 transistors and discussions with Western Electric people. These parameters are being used in the design of new basic circuits.

The Western Electric GF-45011 transistor is the production version of a Bell Telephone Laboratories 2039-2. This transistor is characterized by having an α which is greater than 0.93 and a reverse emitter-to-base breakdown voltage of 4v. These improved characteristics over the earlier diffused-base transistors make it possible to eliminate the diodes placed in the emitter circuit of previous flipflop circuits and considerably improve the tolerance limitations by permitting more circuits to be put in cascade or allowing bigger signals to be considered as standard for most flipflops.

It was decided that the first and most useful flipflop design on which much effort should be spent is the non-symmetrical last moving point flipflop. A routine is being written for Illiac to analyze such a design in hopes of attaining a fast, low gating current flipflop.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. Circuit Design

One reason that speed-independent designs of the arithmetic unit may be slower than corresponding asynchronous designs which are not speed-independent is that in the speed-independent designs it was necessary to combine completion signals from all flipflops into a single completion signal which then had to be amplified so that it could drive gates in all the stages. This amplification might be expected to take a time comparable to gating and other operations, and since it was performed after gating, the times were additive.

A new design has been obtained which should be applicable to most of the arithmetic unit which permits the overlapping of this operation with the gating and, hence, represents a correspondingly faster circuit. This design, however, requires the use of additional C-elements and its speed and effectiveness will depend upon the possibility of obtaining a cheap and fast C-element.

2. Transit Time Investigation

An investigation has been made of the logical problems associated with delay line storage of information. Of particular interest are the problems associated with high speed processing of information in such synchronous systems. An example was used in order to obtain a better understanding of the nature of these problems. This example consisted of a logical machine which was capable of mimicking the behavior of any arbitrary machine. The design of the universal machine depends on a parameter n, which depends, in turn, upon the complexity of the machine being imitated. Several designs were made, some of which tended toward economy in equipment and some of which tended toward increased speed of operation. An effort is being made to find a way of describing the timing problems as concisely as the logical problems are described at present.

3. Alternative Approach to Asynchronous Circuit Theory

An alternative approach has been made to the theory of asynchronous circuits in which the behavior of a circuit is described by a matrix of transition probabilities between states. This theory should be amenable to generalization so as to include the possibility of arbitrary malfunctions. When probabilities corresponding to malfunctions are made zero it should specialize to the existing theory. Definitions for speed independence and semi-modularity have already been re-expressed.

PART III

MATHEMATICAL METHODS

1. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

X-12 Symbolic Address Decimal Order Input. This is a versatile input assembly program which replaces Routine X-1 (Decimal Order Input) as the standard routine for the input of programs. Although it retains all the features of X-1, it also permits the programmer to use symbolic addresses to refer to words in his program. Such symbolic addresses are written as any combination of teletype characters placed between parentheses. Library routines stored permanently on the drum may be compiled by means of this routine where such library routines are referred to by symbolic addresses corresponding to their library designations. The entire assembly program operates by recording a preliminary version of the assembled program on the drum. A second pass is made after input is completed and the final version of the assembled program is played back into the Williams memory.

Y-4 Input Routines to Drum. This program, which replaces the older routine Y-3, may be used to record library routines on the drum so that they may be compiled in arbitrary Williams memory locations. Although relative address terminations and pre-set parameter terminations are preserved, the recorded program is usually more compact on the drum than when it is placed in its final form in the Williams memory. This routine has been used for recording several library routines in the non-erasable part of the drum in such a form that they may be obtained by use of S.A.D.O.I.

Q-5 Complete Circuit Analyzer. This routine performs the same sorts of tests as Q-3 and Q-4 but has a larger capacity since it uses

the drum for storage of concurrent states. It is also capable of testing more complicated circuits since it uses two words rather than one to represent a state.

2. Flows behind Shocks (This work is supported in part by National Science Foundation under Grant G2794.)

Further coding and testing of methods of integrating the Eulerian form of the equations of hydrodynamics has been carried out.

3. Numerical Methods (This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

A program which produced a table for converting order pairs to fractions was written and run. Copies of the table are available.

A complete program which uses the drum for computing eigenvectors and/or eigenvalues of a real symmetric matrix by the Jacobi method is being written. The program will handle matrices of order less than 66.

It is anticipated that this program will be considerably slower than the program using Givens' method. It is hoped that tests of their relative accuracy and, eventually, of their relative merits if eigenvectors are also sought can be run.

A complete program for converting subroutines written using symbolic address to Decimal Order Imput form has been written. The program is intended to be used only in the preparation of library routines.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During July specifications were presented for 14 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1024T. Numbers followed by T are for theses.

1024T Physics. Electron Orbit Evaluation. The computation of electron orbits in a certain type of magnetic field is required for the design of an electron spectrometer.

1025T Psychology. P-technique Factor Analysis of a Maladjusted Mental Defective. A maladjusted mentally defective hospital patient was measured on 42 variables. The variables were chosen in the hope that their factor structure would permit inferences to be drawn concerning the subject's motivational structure. This places factor analysis in the role of an objective psychoanalysis. The intercorrelations of the 42 variables will be factor-analyzed and rotated for simple structure on ILLIAC.

1026T Structural Research. Beam Column Investigation. This problem concerns a beam column investigation of a particular cross-section. The moment and thrust that the beam can sustain with a given strain distribution on the cross-section are to be determined. Mathematically, the problem is one of evaluating several algebraic functions in terms of the conditioning parameters.

1027T Theoretical and Applied Mechanics. Discontinuity Stresses at Sphere-Cylinder Intersection. The discontinuity stresses at the juncture between a spherical and a cylindrical shell structure subject to internal pressure are to be analyzed. The stress-concentration factor as a function of shell thicknesses, mid-surface radii and elastic properties of the material is also to be determined.

1028 Theoretical and Applied Mechanics. Euler Buckling Loads. The collapse of cylindrical shells under external pressure will be investigated. The results will consist of the buckling pressures for various combinations of ratios of length to radius and shell thickness to radius. These results will be used to check a proposed theory.

1029 Physics. Compiler for Illiac. This compiler will permit the use of a simplified multiple address pseudo order code with Illiac. Provision will be made for automatic cycling and address modification. It will use fixed point arithmetic.

1030 Computer. Modification of A-4. The 1.7 precision, floating binary routine A-4 is to be revised so that it will use the same pseudo-order code as the standard floating decimal routine A-1.

1031 Chemistry. Radiation Kinetics. This problem is a theoretical investigation of the kinetics involved in the irradiation of water solutions. Both diffusion and chemical reactions are taken into account. A program is to be written initially for the spherically symmetric case and if this is successful it will be followed by one in which two space variables are used.

1032 Physics. Boltzmann Equation. A solution of the Boltzmann equation of state for electrons in a semiconductor is desired. The electrons are regarded as interacting with both acoustical and optical phonons

1033 Theoretical and Applied Mechanics. Launcher Dynamics Study. An investigation will be made of the dynamic response of rocket launchers during the launching period and the effect this might have on the behavior of the rocket immediately after launching. For this purpose the physical problem is reduced to consideration of some kind of spring-supported beam under the influence of a moving mass load.

1034 Chemistry. Quantum Mechanical Theory of Reaction Rates. This program represents a revision of the wave packet problem described under number 1014. By using a different type of wave packet it is hoped that a reduction in computation time can be achieved.

1035 Physics. Carbon Resistor Temperature Calibration. A least squares fit will be made to determine a formula for the resistance of a carbon resistor as a function of temperature in the range 1 to 8 degrees Kelvin.

1036 Civil Engineering. Characteristics of Time-Speed Variation in Vehicular Speeds. This study is part of a long-range research project investigating characteristics of vehicular speeds on Illinois highways. As a guide for future sampling techniques, as well as for immediate information, project personnel desire to determine characteristics of speed variation over short time intervals within a 24 hour period. A statistical study will be made of these variations.

1037 Theoretical and Applied Mechanics. Large Deflections of Simply Supported Circular Elastic Plates Subjected to Axial Edge Loads. Exact solution for the large deflections of a simply supported circular plate with a concentric hole subjected to axial edge loads will be sought. The solution is applicable to thin elastic plates.

Table I shows distribution of machine time for the month of July.

	Hrs:Min.
Regular Maintenance	33:21
Unscheduled Maintenance	13:07
Drum Engineering	53:49
R.A.R.	4:39
Leapfrog	46:50
Wasted	:00

Use by Departments

	Hrs:Min.
Computer	37:22
Physics	14:44
Control Systems Lab.	61:18
Structural Research	17:45
Structural Res. (AF 24994)	40:10
Structural Res. (AF 170)	:04
Structural Res. (AF 3203)	4:58
Theor. & Appl. Mech. (NR 1834 (14))	2:41
Theor. & Appl. Mech. (ORD 593 IC)	:58
Psychology (M D 620)	:24
Psychology	26:41
Electrical Engineering	25:23
Elec. Eng. (AF 33(038)28634)	:04
Elec. Eng. (AF 3220)	2:20
Chemistry	83:02
Agriculture	16:40
Demonstrations	:15
Miscellaneous	45:55
	532:30

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next

day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for July.

TABLE III

Adder	2
Reader	3
Memory	2
Drum	6
Scope	3
Total	16

One of the adder errors was actually nine errors before it was found and corrected and one of the drum errors was actually six errors before it was found and corrected.

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
7/1/57	19:56	:04	1	(1) Drum error	:00	1:13	0
7/2/57	20:00	:00	0		:00	:45	0
7/3/57	20:00	:00	0		:00	1:10	0
7/5/57	20:00	:00	0		:00	1:50	0
7/8/57	19:59	:01	1	(1) Scope error	:00	:52	0
7/9/57	19:54	:06	2	(1) Data tape tore in reader K (2) Drum error	:00	:52	0
7/10/57	18:47	1:13	2	(1) Drum error (2) Leapfrog failure (start of a series of 9 errors due to a 6BQ7 in adder, V30, with intermittent shorts)	:00	2:35	1
7/11/57	18:35	1:25	0		:00	3:10	0
7/12/57	18:45	1:15	0		:00	1:21	0
7/15/57	19:22	:38	0		:00	1:24	0
7/16/57	17:58	2:02	1	(1) Scope error	:00	:40	0
7/17/57	18:01	1:59	0		:00	1:38	0
7/18/57	16:02	3:58	1	(1) Drum error (start of a series of 6 drum synchronization errors which was corrected finally on July 23 after checking a number of tubes)	:00	:43	0
7/19/57	19:55	:05	1	(1) Drum error	:00	:40	0
7/22/57	18:59	1:01	0		:00	:24	0
7/23/57	19:39	:21	2	(1) Leapfrog failure memory 2^{-32} (2) Scope error, film not advancing	:00	1:31	1

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
7/24/57	20:00	:00	0		:00	1:11	0
7/25/57	17:53	2:07	1	(1) Leapfrog failure, long carry type failure memory position 2^{-28}, 2^{-29}	:00	1:52	1
7/26/57	18:47	1:13	1	(1) Leapfrog failure. Memory 2^{-35}	:00	:31	1
7/29/57	19:57	:03	1	(1) Drum error	:00	1:06	0
7/30/57	20:00	:00	0		:00	:42	0
7/31/57	19:58	:02	2	(1) Reader K error (2) Reader K error	:00	:56	0
TOTALS	426:27	17:33	16		:00	27:06	4

Personnel

The personnel associated with the group and hence the contributors to this report are:

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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

Part I: Study Program on High-Speed Computer

Part II: Illiac Use and Operation - General Laboratory Information

(Most vacations in the Digital Computer Laboratory are being taken during the months of August and September.)

August, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. Feasibility Study Report

The bulk of the staff has been engaged in the preparation of a report summarizing the material which has been presented in these monthly reports during the past year. This report will be available under the title "On the Design of a Very High-Speed Computer".

2. Gating of Non-Symmetrical Flipflops

The methods of gating flipflops were investigated as applied to shifting registers. Two different schemes seem best suited to shifting registers, in an attempt to use few or no transistors in the gating logic.

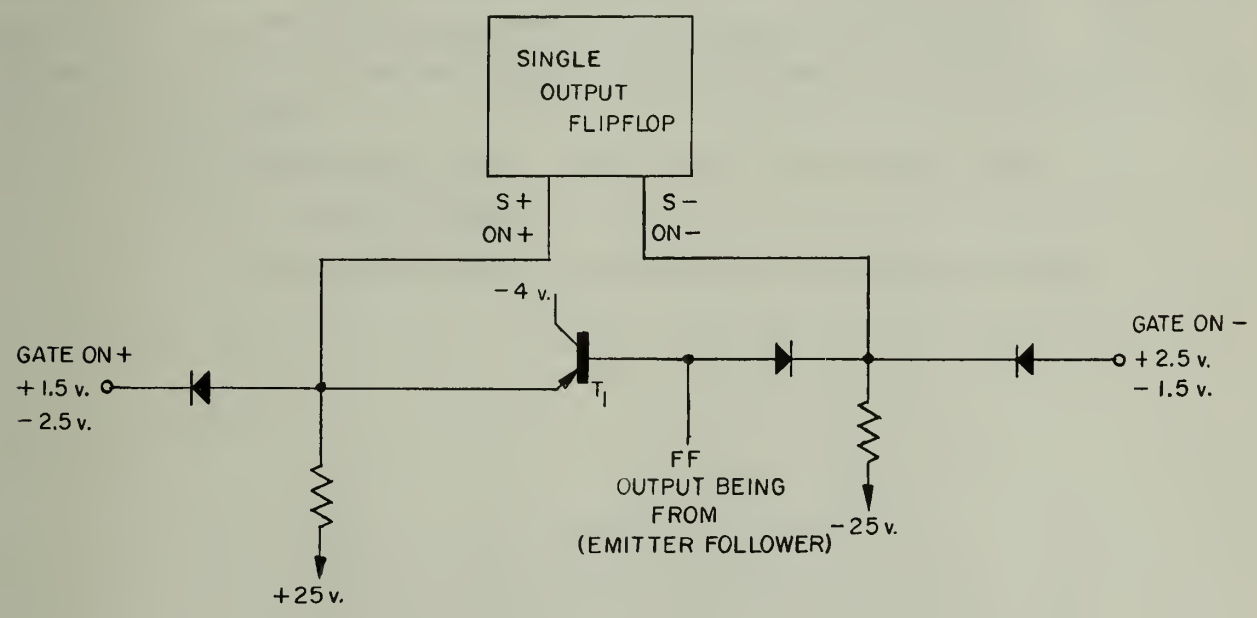

Figure 1

The first method shown above effectively is an AND and an OR circuit for the gating. Two inverse gate drive signals are required. For a shift register with 2 flipflops and 6 gates per digit, we need 12 transistors and 26 diodes per digit. This does not include any gate driver requirements. The second method is to use a diamond gate configuration into a non-symmetric flipflop.

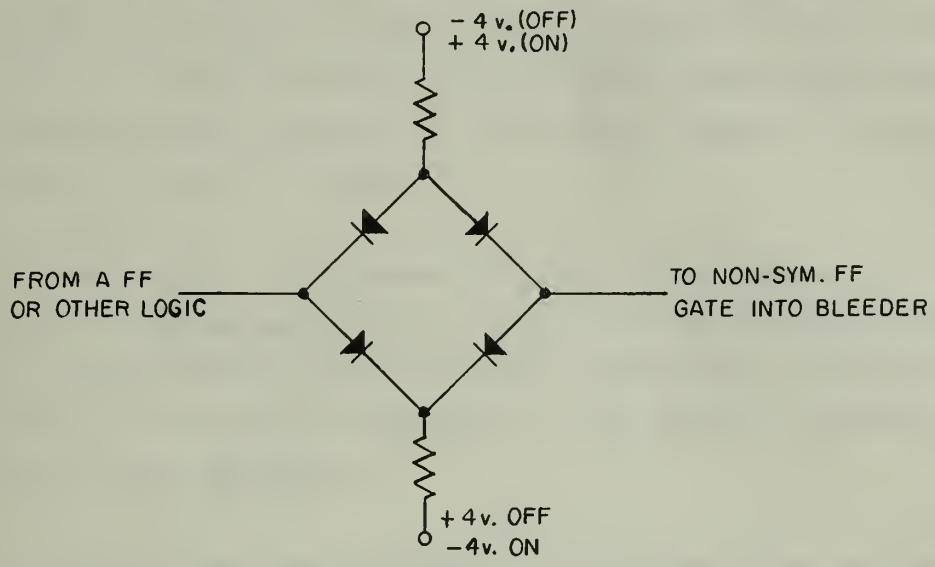

Figure 2

The advantage of such an arrangement is that 4 diodes accomplish the double gating procedure. For a shifting register with 2 flipflops and 6 double gates per digit, we need 312 transistors and 1456 diodes for 52 digits. This is 6 transistors and 28 diodes per digit. These estimates do not include any gate driver requirements.

The disadvantages which might apply to the diamond gate are:

1. It may be slow.
2. The driver requirements may be difficult to supply.

PART II

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During August specifications were presented for 15 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1038T. Numbers followed by T are for theses.

1038 T Civil Engineering. Development of Least Weight Proportions for Variable-Length Trusses. A determination will be made of the least weight proportions of Pratt trussed double-cantilever type aircraft hangers with a secondary roof truss structure. This will be done by obtaining a large number of different designs using different design parameters.

1039 Digital Computer Laboratory. Studies in Floating Point Arithmetic. A study will be made of the loss of accuracy resulting from different systems of standardization in floating binary arithmetic. Linear systems involving nearly singular matrices will be used in this study.

1040 T Chemistry. Effective Isotopic Substitutions in the Rates of Chemical Reactions. A least squares study will be made of the temperature dependence of the ratio of rate constants for reactions involving molecules of different isotopic species.

1041 Structural Research. An Analysis of Deflecting Frames. Final moments and relative story deflections of multi-story, multi-bay frames given fixed-end moments, relative stiffnesses and the position of hinge ends will be obtained.

1042 Psychology. Relationship of Parent to Child Behavior in Problem and Non-Problem Children. A preliminary factor analysis will be made of data obtained by interviewing and testing 30 families with well-adjusted children and 30

families with children having emotional problems. It is hoped that from this study a relevant set of variables may be obtained for studying effects of parental behavior on child behavior.

1043 Chemistry. Self-Consistent Field Calculations of Ions, Atoms and Molecules. Wave functions and energies having electrons in potentials which are not spherically symmetric are to be computed using the methods of Illiac Library Routine F-4.

1044 Electrical Engineering. Effective Carrier Mobility. By considering scattering from a surface potential well, a theoretical expression has been found for the effective mobility of current carriers, in the surface layer of a semiconductor, as a function of parameters describing the surface conditions of the semiconductor. Presently available calculations will be checked and extended by use of the Illiac.

1045 Psychology. A Comparison of Two Personality Inventories and Personality Correlates of Conditionability. A comparison of the factor structures of the Cattell 16 personality factor inventory and the Guilford 13 personality factor inventory will be made by statistical techniques. Also Eysenck's hypothesis that a characteristic of the nervous system, termed reactive inhibition, is the basis for personality differences, termed extraversion-introversion, will be checked. This checking will be done by a multiple factor analysis.

1046 Structural Research. Miscellaneous Studies of Vibration of Plates, Stresses in Buildings due to Violent Ground Motion or Blast Forces. Straight dams subjected to earthquake tremors may be approximated by plates having concentrated mass points which are subjected to vibrations at the edges. Shearing and flexural stiffness is assumed. Numerical integration will be carried out using a small time interval.

1047 Animal Science. Weather Effects on Milk Production. To seek weather effects on milk production, the shape of the lactation curve of the individual cow and lactation must be taken into account. This will be done by calculating

fitted quadratics (already shown to be adequate) and accumulating deviations separately for each of several days, the accumulations presumably containing the effects of weather.

1048 State Water Survey. Probability of Extreme Values in Illinois Rainfall. Least squares fitting will be made of several different linear functions to 1-day, 2-day, 3-day, 5-day, 10-day annual maximum rainfall amounts from 39 stations with 40 years of records.

1049 Structural Research. A Numerical Analysis for Elastic and Elasto-plastic Frames. The problem consists of finding the static joint moments and story deflections of a multi-story and multi-bay frame subjected to an initial imposed loading, and the successive plastic hinge formation due to an added pattern of incremental loads. Plastic hinge formation is assumed to occur only at the joints and the collapse condition is not specified.

1050 Theoretical and Applied Mechanics. Mechanical Vibration Filters with Nonlinear Characteristics. A study will be made of a single degree of freedom system with nonlinear spring and damping characteristics represented by the equation

$$m\ddot{x} + c|\dot{x}|^{n-1}\dot{x} + P_0 \tanh\left(\frac{h_0 x}{P_0}\right) = a_0\omega^2 \cos \omega t \ .$$

1051 T Psychology. A Factor Analysis of Concepts used in Self-Description. Sixty-six undergraduate students at the University of Illinois were asked to make judgements concerning the degree to which certain words were descriptive of them. The product-moment correlation was then calculated for every word with every other, yielding a 30 x 30 matrix. The next step in the analysis of these data involves the decomposition of this matrix of intercorrelations into statistically independent factors.

1052 Student Counseling Service. Prediction of Academic Success at the University of Illinois (Chicago). Data have been secured for 3,012 Chicago Undergraduate

Division students on 27 tests and other predictors which it is thought may be related to academic success at the University. Criterion data have been secured in the form of grade point averages for the first semester, plus a number of different measures of academic survival for the first semester. Selected multiple correlations are to be secured (with beta weights and standard errors of beta weights) as a basis for choosing several different combinations of predictors which will give near-maximal predictive efficiency for predicting college success.

Table I shows distribution of machine time for the month of August.

Table I

	Hrs:Min.
Regular Maintenance	25:51
Unscheduled Maintenance	5:09
Drum Engineering	53:12
R.A.R.	5:35
Leapfrog	38:12
Wasted	:05
<u>Use by Departments</u>	
Computer	43:18
Physics	19:53
Control Systems Lab.	45:30
Structural Research	34:53
Struct. Res. (AF 24994)	50:28
Struct. Res. (AF 2303)	:06
Theor. and Appl. Mech. (ORD 593 IC)	3:46
Theor. and Appl. Mech. (Task 14)	1:52
Psychology	19:25
Psychology (Dept. Pub. Welfare)	2:21
Electrical Engineering	27:04
Elec. Eng. (AF 3220)	:03
Elec. Eng. (AF 1310)	1:12
Chemistry	74:47
Agriculture	34:48
Demonstrations	1:17
Miscellaneous	53:20
	542:07

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for August.

Table III

Control Errors	1
Memory Errors	1
Drum Errors	6
Reader Errors	7
Punch Errors	4
Unknown	1
Total	20

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
8/1/57	17:48	2:10	1	(1) Drum failure *	:02	1:18	0
8/2/57	17:38	2:22	2	(1) Drum failure (2) Drum failure	:00	:42	0
8/5/57	19:57	:03	3	(1) Unknown (2) Punch punched extra 2 holes Punch No. 3 (3) Punch failure Punch No. 4	:00	:54	0
8/6/57	19:59	:01	1	(1) Punch error Punch No. 4	:00	:48	0
8/7/57	19:29	:31	1	(1) Drum failure **	:00	:47	0
8/8/57	19:10	:50	1	(1) Control error **	:00	:41	0
8/9/57	20:00	:00	0		:00	:44	0
8/12/57	19:39	:21	1	(1) Leapfrog failure, memory error 2^0	:00	1:10	1
8/13/57	19:59	:01	1	(1) Reader error Reader K	:00	:54	0
8/14/57	19:57	:03	3	(1) Unknown (2) Unknown (3) Unknown } Possibly reader error. Reader K	:00	1:38	0
8/15/57	19:59	:01	1	(1) Drum failure	:00	:44	0
8/16/57	20:00	:00	0		:00	:45	0
8/19/57	19:59	:01	1	(1) Possibly reader error Reader K	:00	:46	0
8/20/57	19:34	:26	3	(1) Leapfrog failure. Punch error Punch No. 4 (2) Reader error Reader K (3) Reader error Reader K	:00	1:22	1
8/21/57	20:00	:00	0		:00	:41	0
8/22/57	20:00	:00	0		:00	:40	0
8/23/57	20:00	:00	0		:00	:40	0

TABLE II (Continued)

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
8/26/57	20:00	:00	0		:00	:46	0
8/27/57	19:58	:02	1	(1) Drum failure	:00	:48	0
8/28/57	20:00	:00	0		:00	1:05	0
8/29/57	19:57	:00	0		:03	2:00	0
8/30/57	20:00	:00	0		:00	:58	0
				* A part of repair time this day was used trying to find original drum error. ** Repair time all for drum failure of 8/7/57.			
TOTALS	433:03	6:52	20		:05	20:51	2

Personnel

The personnel associated with the group and hence the contributors to this report are:

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The work of the group is under the administration of an Executive Committee with the following members: N. M. Newmark, Chairman, D. E. Muller, D. B. Gillies, J. E. Robertson, A. H. Taub, and R. E. Meagher.

UNIVERSITY OF ILLINOIS
GRADUATE COLLEGE
DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

PART I: STUDY PROGRAM ON HIGH-SPEED COMPUTER

PART II: SWITCHING CIRCUIT THEORY

PART III: MATHEMATICAL METHODS

PART IV: ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

September, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. The Summary Report

A summary report on the design of a computer has been completed and issued as Digital Computer Laboratory Report No. 80 entitled "On the Design of a Very High-Speed Computer". The summary and conclusions of this report are reproduced here:

"On the basis of the work reported herein the Digital Computer Laboratory of the University of Illinois concludes that it is feasible to construct a very fast digital computer in which the transistor circuits developed in that Laboratory would be used.

The results of two design studies are discussed. One involves a minimum of buffer storage in the form of transistor registers and is outlined in the body of Chapter 3 while the other involves a moderate amount of buffer storage in the form of a small-capacity, high-speed, random-access buffer memory and is discussed in the appendix to Chapter 3. The former design is emphasized because it is felt that its equipment requirements can be presently met.

In it two controls are used, arithmetic control and advanced control, as well as buffer storage for instructions and operands, and by such means various units of the computer are kept in simultaneous operation. For example B-modifications, memory accesses and complicated arithmetic operations such as a double-length, add-product instruction may be performed concurrently. Short but powerful inner loops may be stored outside the memory and acted upon by the control. Many of the gains in speed in the control and arithmetic unit are dependent upon asynchronous operation of these units.

The relative speed of the proposed computer compared to that of existing machines depends upon the problem being solved. For problems dominated by arithmetic operations it is estimated that the proposed computer will be 100 to 200 times faster than computers such as Illiac. For problems dominated by logical and combinatorial operations, this factor of gain in speed will be at least 50.

The proposed computer has a random-access word-arrangement memory of 8192 words of 52 bits each with an access-time of 1.5 μs.

The arithmetic unit is designed so that the digits of a multiplier are sensed and acted upon in such a way that the use of the adder is reduced. Furthermore "carry registers" are used in this unit and carries are assimilated only when necessary. It is expected that the proposed computer will have an average multiplication time between 3.5 and 4 μs, addition times (with assimilation) of .3 μs and division times of 7 to 20 μs.

The computer, aside from input-output facilities, will contain approximately 13,000 transistors, 38,000 diodes, and 42,000 resistors. The transistors are expected to be Western Electric transistors, type GF-45011.

The basic circuits built from these transistors have operation times of from 5 to 40 x 10^{-9} second depending upon the circuit."

2. Transistor Procurement and Testing

Nine Western Electric GF-45011 transistors were received and tested during the month. Preliminary plans were made for a production-type transistor tester in anticipation of receipt of several hundred transistors.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

The techniques for designing distributive circuits are being applied to the design of the control of the computer described in Digital Computer Laboratory Report 80. These techniques were described in previous progress reports. They have been used, to date, only in the design of relatively simple circuits, and the purpose of the present effort is to learn more about the difficulties involved in using them to design a relatively complicated circuit.

A partially ordered set of C-signals is set down as the initial description of the behavior of the circuit. Here, the C-signals correspond to operations which are to be performed by the circuit and the ordering relations between them correspond to chronological ordering or "causation" relations between these operations. The setting down of a chart of such operations and relations presupposes a given initial state of the circuit. In practice, however, one wishes to design circuits having variations of behavior corresponding to many initial states. To take account of such variations of behavior with the present techniques would require that a separate partially ordered set of C-signals be given for each initial state. Such a multiple listing would be prohibitive in practice, and for this reason an attempt has been made to condense all of these descriptions into the form of a single chart.

One way of achieving such a condensation is to associate each ordering relationship with the conditions under which it is valid. Thus, if the ordering relationships are represented by directed lines on the chart, one may write a Boolean condition above each which is required for its validity.

A second technique is also used to simplify the resulting chart. This involves relaxing the condition (File No. 225, page 6, point C) that if a C-signal (α,i) is in Σ, the set of C-signals, and $\alpha>1$, then $(\alpha-1,i)$ is also

in $\leq$ and $(\alpha-1,i) \leq (\alpha,i)$. If one replaces this with the weaker condition that if (α,i) and (β,i) are both in $\leq$ and $\beta \leq \alpha$ then $(\beta,i) \leq (\alpha,i)$, one achieves a certain arbitrariness in the selection of the integers α and β corresponding to given operations. No weakening of the theory is actually produced by this change, and yet it becomes possible to make many simplifications in a composite chart of the type required to describe a complicated circuit.

Thus, experience in the design of a complicated circuit has led to the adoption of two new techniques to facilitate the handling of composite charts representing the behavior of a circuit under various initial conditions. A more efficient way of describing the handling of information is still being sought. It is also hoped that a consequence of such a method would be some way of determining which of the ordering relations among the various operations in any given description are required for the correct functioning of the circuit and which may be eliminated.

PART III

MATHEMATICAL METHODS

1. Program Library. (Supported by Office of Naval Research under Contract N6ori-07130.)

T-6 Fast Arcsine. This program uses an expression of the form

$$\sin^{-1} x = cx + \frac{a \cdot x \cdot |x|}{b - |x|}$$

to obtain values of $\sin^{-1} x$ in the range 0 to 84° which are accurate to better than a degree. Only 2.6 milliseconds are required for the calculation.

2. Numerical Methods (This work is supported in part by the Office of Naval Research under Contract N6ori-07130).

A program for finding eigenvalues and vectors has been completed which will handle matrices up to order 65. This new routine uses the drum for storage. It uses the method of Givens to obtain eigenvalues and an extension due to Wilkinson to obtain the vectors. In Wilkinson's method the eigenvectors of the tri-diagonal form are found, and a subsequent rotation by the transformation matrix gives the eigenvectors of the original. This program has the disadvantage that the vectors will not be orthogonal unless the eigenvalues are distinct.

A comparison of the speed of the present program and that of a program using the Jacobi method is given in the following table of times. In the limit of a 65th order matrix the Jacobi method is estimated to be slower by a factor of 3.

Order	Times (mins. and secs.) Jacobi	Givens-Wilkinson
5	00.20	00.30
10	01.30	01.40
15	04.10	03.40
30	27.45	15.30
45		41.00
55		64.00

Assuming the time is a function of the form $an + bn^2 + cn^3$, where n = order of matrix, the following coefficients were calculated.

	Jacobi	Givens-Wilkinson
a	.03	.096
b	.003	.00764
c	.000903	.000213

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During August specifications were presented for 7 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1053. Numbers followed by T are for theses.

1053 Animal Science. Fitting "Bent Straight Line". It is frequently necessary to fit a line to data from nutrition and other biological experiments which hypothetically follow a straight line in the first part of the range of absiccas and, continuous with this line, another straight line (that is, another slope) for the rest of the range of abscissas. This problem will be solved by the computer because the abscissa of the bend point is a nonlinear function of the data in the normal equations.

1054 T Computer. Design of Circuits from a Tolerance Viewpoint. A Monte Carlo method is used to evaluate successive steps in a synthesis of circuits with component tolerances. A statistical approach is used throughout the problem to arrive at the solution which has the highest probability of satisfactory performance.

1055 Student Counceling Bureau (Chicago). Prediction of Academic Survival. All freshmen at the Chicago Undergraduate Division are given a battery of tests to determine academic survival. This type of analysis is a recurrent one since it is desirable to ultimately arrive at a method of accurate prediction.

1056 Computer. Last Moving Point Flipflop Analysis. A number of linear algebraic equations are solved giving output voltages, currents and powers of a two-transistor last moving point flipflop. The variables used in the equations are tolerances, power supply voltages, resistor values, and diode and transistor characteristics.

1057 Psychology. Personality Structure Verification and Measurement. In order to develop more highly saturated measures of objective test personality factors, Pearson product moment correlations will be obtained of intact tests with estimates of the factor score and of single digit test item scores with estimates of factor scores.

1058 Dairy Science. Analysis of Growth and Production Data from Crossbreeding. Milk and fat production data and growth data will be used to evaluate the effects of various breeding factors.

1059 Psychology. Language Community Factor Structure. Data in the form of semantic evaluations of nonlinguistic signs has been gathered from three separate language groups (Spanish, English and Navajo). It is proposed that each of the three separate collections of data be analyzed to determine the presence or absence of similarity of factor structure for these data from the language groups.

Table I shows the distribution of machine time for the month of September.

Table I

	Hrs:Min.
Regular Maintenance	24:56
Unscheduled Maintenance	:54
Drum Engineering	42:48
R.A.R.	5:09
Leapfrog	41:35
Wasted	:02
<u>Use by Departments</u>	
Computer	28:57
Physics	4:56
Control Systems Lab.	64:18
Structural Research	119:55
Struct. Res. (AF 24994)	25:45
Theor. and Appl. Mech. (ORD 593 IC)	:03
Psychology	15:29
Electrical Engineering	3:28
Chemistry	54:26
Agriculture	19:17
U.S. Dept. Public Health	:50
Ill. Dept. Public Welfare	:08
Miscellaneous	33:10
Demonstrations	:14
	486:20

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a num ber of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for September.

TABLE III

Control Errors	3
Punch Errors	1
Drum Errors	6
Scope Errors	1
Unknown	2
Total	13

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
9/3/57	20:00	:00	0		:00	:41	0
9/4/57	19:58	:02	2	(1) Possibly white switch trouble (control) (2) Light out on "B" gate punch No. 4	:00	1:12	0
9/5/57	20:00	:00	0		:00	1:50	0
9/6/57	20:00	:00	0		:00	:47	0
9/9/57	20:00	:00	0		:00	1:14	0
9/10/57	20:00	:00	0		:00	1:00	0
9/11/57	18:07	1:53	1	(1) Head connector in cable to track 288 of drum shorted.	:00	:26	0
9/12/57	20:00	:00	0		:00	1:06	0
9/13/57	20:00	:00	0		:00	:42	0
9/16/57	19:44	:16	3	(1) Drum error (2) Drum error (3) Drum error	:00	1:09	0
9/17/57	19:37	:23	2	(1) Unknown (2) Drum error	:00	:50	0
9/18/57	19:59	:01	1	(1) Control error (?)	:00	:53	0
9/19/57	19:59	:01	1	(1) White switch trouble (control)	:00	1:00	0
9/20/57	20:00	:00	0		:00	:40	0
9/23/57	19:33	:27	1	(1) Unknown	:00	1:48	0
9/24/57	20:00	:00	0		:00	3:20	0
9/25/57	20:00	:00	0		:00	:39	0
9/26/57	20:00	:00	0		:00	1:02	0
9/27/57	19:57	:01	1	(1) Drum error	:02	:40	0
9/30/57	19:59	:01	1	(1) Scope error (film jammed)	:00	2:31	0
TOTALS	396:53	3:05	13		:02	23:38	0

Reports and Seminars

Seminars

"Storage and Switching by Magnetic Elements," by Dr. Jan A. Rajchman RCA Research Laboratories, September 24, 1957.

Personnel

On May 28, 1957 the University Board of Trustees voted that the Digital Computer Laboratory be a department in the Graduate College effective September 1, 1957. R. E. Meagher was appointed Head of the Laboratory. The Department Advisory Committee consists of Professors L. D. Fosdick, D. B. Gillies, D. E. Muller, W. J. Poppelbaum, J. E. Robertson, J. N. Snyder, and A. H. Taub.

The personnel associated with the department and hence the contributors to this report are:

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Carter, Clifford E., Electronics Engineer for Illiac
Clark, Miss Helen B., Secretary
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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

PART I: STUDY PROGRAM ON HIGH-SPEED COMPUTER

PART II: SWITCHING CIRCUIT THEORY

PART III: MATHEMATICAL METHODS

PART IV: GENERAL RESEARCH

PART V: ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

October, 1957

PART I

STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. At(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition, this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. Arithmetic Unit

Carry Propagation Study

The problem of determining the expected maximum carry propagation when adding random numbers using various logical designs was investigated. This problem is of interest for:

(A) Illiac-type adders modified for a carry completion signal, when the adder is of length $n \geq 40$ stages. Burkes, Goldstine, and von Neumann give recursive probability equations for the maximum expected carry. These equations easily generalize for joint propagation of carries or zero-carries. These equations have been evaluated on Illiac for $40 \leq n \leq 64$ (Problem Specification 1060). A Monte Carlo experiment for $n = 40$ is reported in the literature giving 5.6 stages as the expected value. The Illiac result for $n = 40$ was 5.69.

(B) The type of adder reported in Report No. 80 in which two random numbers x and y are added and two new numbers are obtained, s and c. Carry assimilation then consists of adding s + c and allowing generated carries to propagate. In this problem

$$s_i = (x_i \oplus y_i) \oplus (x_{i+1}\, y_{i+1})$$

$$c_i = (x_{i+1} \oplus y_{i+1}) \cdot (x_{i+2}\, y_{i+2}) \; .$$

A new phenomena occurs which makes a mathematical-probability analysis much more difficult than for (A). When adding s and

c combinations 0,1 or 1,0 <u>propagate</u> while combinations 0,0 or 1,1 <u>initiate</u> a carry or zero-carry. These states are not independent probability-wise from the two preceding states. For example

	i	i+1
s	0	1
c	1	0

cannot occur.

Consequently an analysis must be made of each stage conditional on the two preceding stages.

(C) Carry-borrow type adder discussed in Report No. 81. Given s and c as the sum and carry digits when assimilation is to be performed, the equations have been analyzed sufficiently to yield the following:

Zero-borrow $\quad e_{i-1} = \bar{s}_i(c_i s_{i+1} y_i \vee c_i \bar{s}_{i+1} \vee \bar{c}_i s_{i+1} \vee \bar{c}_i \bar{s}_{i+1} e_i)$

Borrow $\quad x_{i-1} = \bar{s}_i(c_i s_{i+1} f_i \vee \bar{c}_i \bar{s}_{i+1} x_i)$

Zero-carry $\quad f_{i-1} = s_i(c_i \bar{s}_{i+1} x_i \vee c_i s_{i+1} \vee \bar{c}_i \bar{s}_{i+1} \vee \bar{c}_i s_{i+1} f_i)$

Carry $\quad y_{i-1} = s_i(\bar{c}_i s_{i+1} y_i \vee c_i \bar{s}_{i+1} e_i)$

The four Boolean functions so defined are pairwise disjoint and

$$e_{i-1} \vee f_{i-1} \vee x_{i-1} \vee y_{i-1} = 1 \qquad (e_{n+1} = 1,\ f_{n+1} = 0)\ .$$

From these we obtain immediately

Propagating states $\quad \overline{s_i \oplus c_i \oplus s_{i+1}}$

Initiating states $\quad s_i \oplus c_i \oplus s_{i+1}$.

One other interesting relation that may be deduced is:

$$x_{i-1} \vee y_{i-1} = \bar{c}_i(x_i \vee y_i)(\overline{s_i \oplus s_{i+1}}) \vee c_i(\overline{x_i \vee y_i})(s_i \oplus s_{i+1})$$

Floating Point Arithmetic

A double precision, interpretive, floating binary subroutine has been written to experiment with various possible types of wired-in floating point orders for the new computer. This subroutine has an order code which is an extension of the order code of Library Routine A-1, and includes such orders as "standardize the floating accumulator". There are 4096 addressable double precision numbers - numbers with low addresses are held in the Williams memory, and the routine transfers words automatically to or from the drum when necessary. This routine may be easily modified to vary the effective word-length or the standardization procedure to compare various possible computers. It is proposed first to study matrix algebra.

2. Control Studies

Trial Programming

A detailed study of the problems arising in writing the inner loops of two problems has been made. These are the root-finding procedures in Givens' method for the eigenvalues of a symmetric matrix after the matrix has been reduced to tri-diagonal form, and a hyperbolic hydrodynamical problem with 2 space variables and time. In both cases, inner loops existed for which the memory access-time was almost entirely overlapped with arithmetic, and the problem was to find this loop. A useful aid in this search was a chart indicating the partial ordering in time which the various operations have to satisfy. This is a generalization of the idea of a flow chart, since a flow chart generally specifies a unique order for doing operations.

Order Code

A new class of orders have been found, called conditional arithmetic orders. If some arithmetic condition, such as $A \geq 0$, is satisfied, an operation such as "add 1 to the contents of a B-register" is performed. This can save two memory references compared to the two control transfers that would otherwise have to be executed. (Jump out to record the result of the test, and then jump back into sequence.)

3. Core Storage Unit

One-word Unit

The effect of half selection of the switch core on the stored contents of the 50-bit test unit has been investigated experimentally. One of two current drivers was excited continuously by a clock pulse to simulate half-selection of the switch core; the other driver was turned on manually to perform one complete cycle, using a one-shot circuit synchronized with the clock. The following results were obtained:

1. The readout signals did not deteriorate after being disturbed for long periods by the half-selected switch core.
2. The disturbed readout signal was small in comparison to the normal readout signal.
3. Appreciable pickup on the readout wire from the rewrite B-drivers was noted. The amount of pickup to be expected in the full-scale storage unit could not be estimated from the one-word test.

Logical Design

Investigation into the logic necessary for a full-scale memory is being made, and in light of the results, a suitable logic for the test memory is being worked out. At the speeds under consideration for this memory, pulse delay times in the switch core matrix and in the bit core planes themselves, become an appreciable fraction of the access-time. Therefore a careful study must be made of current coincidences within the memory to make sure proper time is allowed for reading and readout. This study has been started and will continue.

Peripheral Circuits

A transistorized pulser was designed and tested; it delivers pulses from 80 mμs to 1 μs apart and is driven by a regenerative amplifier developing sharp edges (for proper triggering from a sine-wave).

More suitable high current drivers were designed. A pair of 6DQ5 power pentodes are used for the output stage of the 0.4 ampere and 0.75 ampere drivers. The UL84, a 12-watt, 100 ma pentode, is used for voltage gain. The

complete driver uses 1 GF-45011 transistor, 2 UL84's, and 2 6DQ5's and generates a 0.4 ampere, 50 mμs pulse from a two-volt input signal after a delay of approximately 50 mμs.

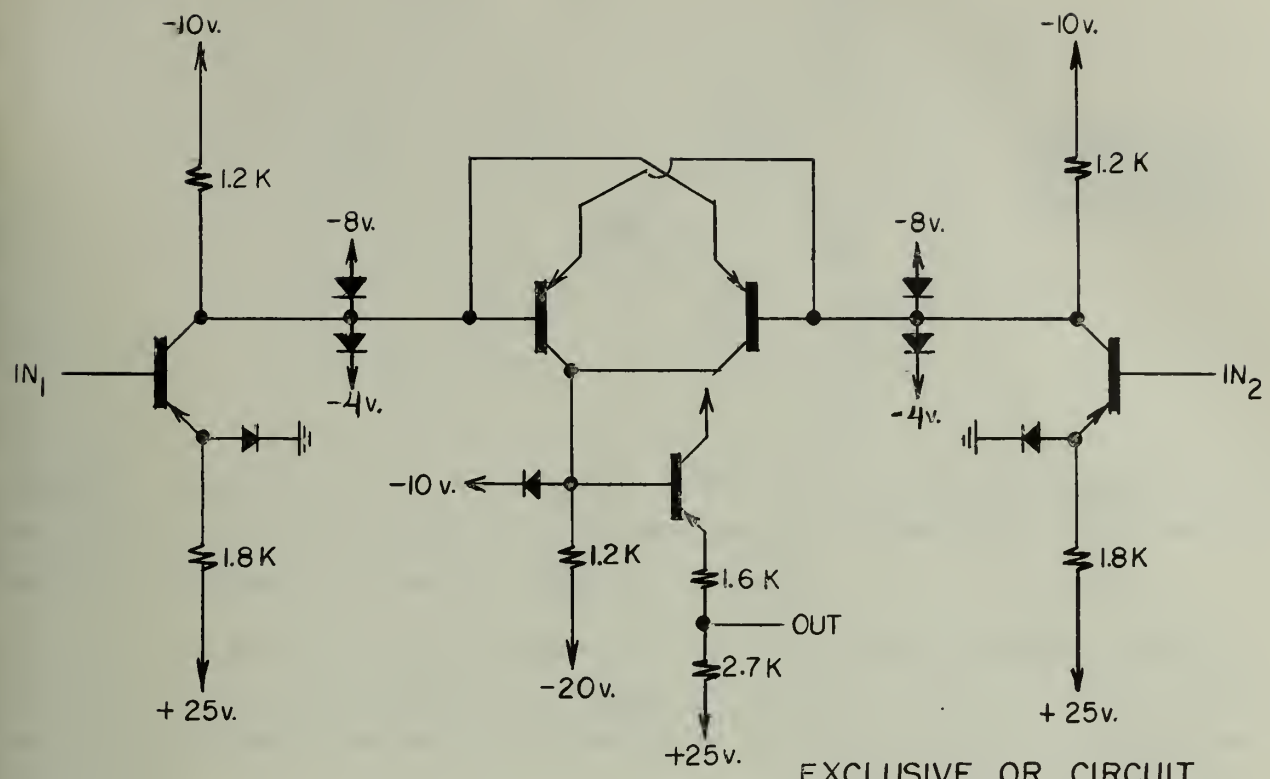
4. Transistor Circuits

Redesign and Tests of the Basic Logical Circuits described in Report 80

Under the first heading come extensive modifications of the flipflops described in Report 80. The principal change was to take the emitter-followers out of the collector-to-base feedback loop and to use them exclusively to drive the outputs from the last moving points. Further changes took account of the increase in the allowed reverse bias on the emitter from 1v to 3v. A minor readjustment of the average emitter-base forward drop figures had also some influence on the new design.

It seems now possible to obtain operation times of 40 mμs and 15 mμs respectively for the symmetric Eccles-Jordan and the Schmidt-Trigger type respectively. As soon as definitive figures are available the circuit values of the new designs will be published.

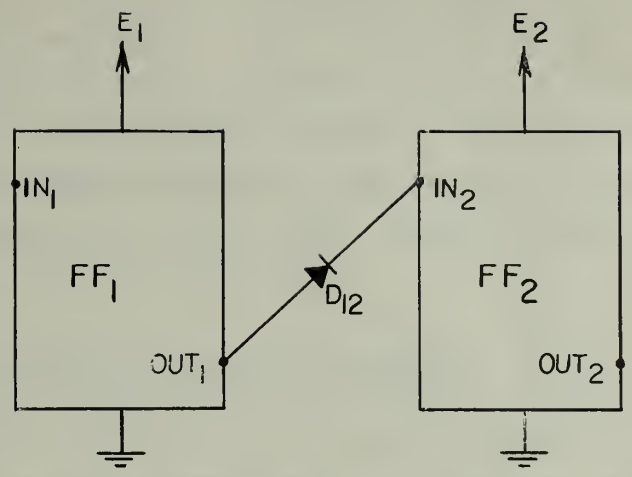
The EXCLUSIVE OR circuit of Report 80 was redesigned in view of obtaining more realistic tolerance conditions. To this end the input inverters were designed to give full swing of the (bumped) collector with inputs between ±0.5v and ±1.5v. The figure below gives the final design which produces under the worst conditions an operation time of 45 mμs. It should be pointed out that this is slower than the one obtainable by the usual half-adder.



EXCLUSIVE OR CIRCUIT

The "Flow-Gating" System

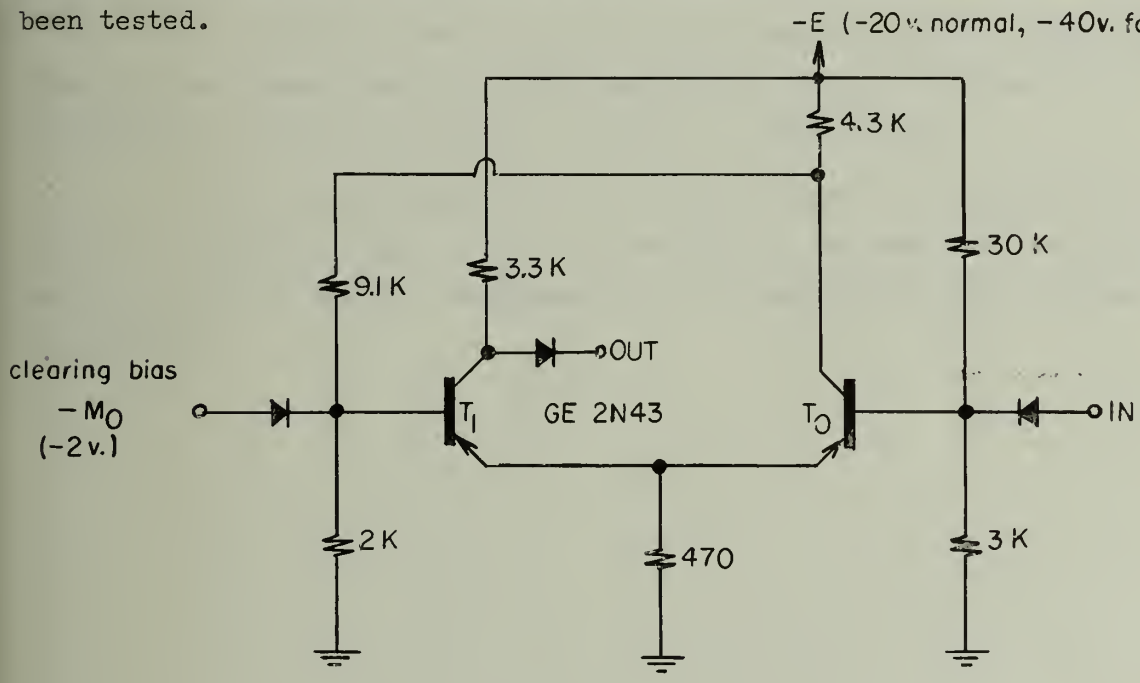
A new principle of information transfer (called "flow gating") was investigated. The fundamental idea can be stated as follows. Consider a flipflop having only one supply voltage (see below for an example) and choose one input and one output such that they are in phase but have a different average potential. Suppose for instance that the average potential of the input is greater than that of the output. We then connect the flipflops with diodes, each diode being always reverse biased as long as the supply voltages E_1 and E_2 (see figure) are the same. No information flows in this case. Now we observe that the state of such a flipflop does not change when we alter the supply voltage since the circuit equations cannot contain E (all currents are proportional to E, the coefficients of proportionality depending on the state!). We now lower the average potential of IN_2 by lowering E_2: at a given moment information will flow through diode D_{12} if flipflop 1 is in the "up"-state, while otherwise flipflop 2 will remain unaffected. If we now continue to clear flipflop 2 to the "down"-state whenever E_2 is lowered (see again below for an



PRICIPLE OF FLOW GATING

example), we have a perfect clearing and gating system using as a coupling element one single diode. Once flipflop 2 has received its information, we can swing E_2 back to the normal value and the state is "trapped".

The make-up of one possible type of flow-gating flipflop is shown in the figure below, the layout being adapted to pnp transistors. Circuit values are only approximate and refer to a prototype the static behavior of which has been tested.



FLOW GATING FLIPFLOP

In the case of the circuit just described, it is easy to see how the clearing and gating comes about. -E is made more and more negative until $-u_0$ holds the base of T_1 at a fixed potential. Suppose that IN is held at a potential below $-u_0$: then T_1 is cut off, driving OUT toward the more negative state. If however IN is at a potential above $-u_0$, the emitter of T_1 will continue to conduct and will also continue to do so as -E goes back to its normal value: OUT will be in its more positive state all the time.

5. Transistor and Diode Procurement and Testing

232 GF-45011 transistors were received during the month of October. A production tester which measures the dc α as well as emitter-base forward and reverse drops (plus some other parameters) was built and is now used to test the incoming units.

About 150 each of Q5-250 and Q10-600 units have been received from Qutronics Semiconductors and have been tested. In general they meet our specifications but tend to have a larger spread of forward drops than did National Union types. Qutronics has agreed to tighten limits and indicates this is quite possible.

The recovery times of these diodes seem to be quite satisfactory. Q5-250 when switched from 10 ma to 5 volts recovers to 250 μa in about 80 mμs. Q10-600 when switched similarly recovers to 600 μa in about 60 mμs.

Certain more general work has been done with the diodes available with respect to recovery time. It is now possible on the basis of one speed measurement to partially predict quantitatively the recovery at other current and voltage conditions.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. Complex switching circuits are generally designed by combining "blocks" consisting of simpler circuits, which are designed individually without regard to their interaction with the whole. Rules for combining such blocks which are semi-modular in such a way as to preserve semi-modularity have been set down in Digital Computer Laboratory Reports 66 and 80, and constitute the basis of a useful synthesis technique.

An alternative to this method of combining blocks is to effect a corresponding combination of the partially ordered sets of C-signals which were originally used to describe the blocks in question. This alternative has two advantages over the block combination method.

(a) The effect upon sequencing of operations is clearer since chronological ordering is expressed directly in the resulting partially ordered set.

(b) A much more general set of rules has been obtained for combining partially ordered sets of C-signals than was obtained for combining circuits. Thus a greater variety of combinations is possible using the alternative method.

All of the rules for combining partially ordered sets of C-signals may be derived without great difficulty from a general theorem describing the conversion of a partially ordered set of C-signals Σ into a contracted set Σ'.

Let Σ be a partially ordered set of C-signals which is realizable as a binary circuit. Then Σ' is similarly realizable if it is formed in the following manner and it is partially ordered.

(1) Place (γ,k) in Σ' if (γ,k) is in Σ, and $k \neq i$, $k \neq j$.

(2) Place (α,i) in Σ' if (α,i) and (α,j) are both in Σ.

(3) Make $(\gamma,k) < (\delta,\ell)$ in Σ' if $(\gamma,k) < (\delta,\ell)$ in Σ.

(4) Make $(\gamma,k) < (\alpha,i)$ or $(\gamma,k) > (\alpha,i)$ in Σ' if $(\gamma,k) < (\alpha,j)$ or $(\gamma,k) > (\alpha,j)$ in Σ.

(5) Include no further ordering relations Σ' except those needed to satisfy the condition of transitivity.

2. Conditions for realizability of a partially ordered set of C-signals in terms of a switching circuit have been set down in an earlier report. It was also shown that these conditions were sufficient for the realization of a binary circuit provided that one is allowed to place additional C-signals in the partially ordered set which correspond to additional circuit elements. This result was proved by exhibiting a particular method for placing such additional elements. A different method for placing such additional elements has now been found which allows one to write down a particularly simple realization of the circuit. This realization requires the use of only four types of logical circuit elements and hence is particularly attractive from the standpoint of electronic circuit design. The required element types are AND, OR, NOT, and C-elements. A C-element is a single output flipflop whose output tends to change only when it disagrees with both inputs. Although such elements have not been designed using high-speed transistors, it seems likely that designs similar to the present single output flipflops are possible.

3. Greater generality has been achieved in the theory concerned with the distributive lattice Λ of C-states used to represent a circuit. This was done by extending the definition of excitation so as to apply to any such lattice derived from a partially ordered set of C-signals, without regard to whether or not it may be realized in terms of a binary or other specific type of circuit.

The required conditions on Λ are:

(i) The elements $\underline{a}$ of Λ must be n-tuples of non-negative integers: $\underline{a} = (\underline{a}_1, \underline{a}_2, \ldots, \underline{a}_n)$.

(ii) They must form a lattice under componentwise ordering in which the least upper bounds and greatest lower bounds are componentwise maxima and minima respectively.

(iii) This lattice contains the zero element whose components are all zero.

(iv) An element $\underline{b}$ covers an element $\underline{a}$ in Λ if and only if for some i we have $\underline{b}_i = \underline{a}_i + 1$ and $\underline{b}_j = \underline{a}_j$ when $j \neq i$.

The extended definition of excitation now reads: Node i is excited in C-state $\underline{a}$ if and only if there exists a C-state $\underline{b}$ which covers $\underline{a}$ and for which $\underline{b}_i = \underline{a}_i + 1$.

The general theorems concerning excitation which were developed in Digital Computer Laboratory Report 78, as well as several subsequent results, may be extended accordingly.

PART III

MATHEMATICAL METHODS

1. Relativistic Field Equations (Supported in part by the National Science Foundation under Grant G2794.)

Work continues on the static spherically symmetric Einstein field equations for a space-time in which a perfect gas at constant entropy exists. A complete set of ordinary differential equations have been derived which take into account the relativistic effects in the determination of the internal energy of the gas as a function of the temperature. These equations will be integrated numerically for various values of central pressure p_c and the constant entropy s. The mass and radius of a spherical distribution of matter will then be determined. Particular attention will be paid to the values of p_c and s for which non-singular solutions of the field equations do not exist and for which the mass as functions of p_c for constant s have maxima.

2. Hydrodynamic Flows with Shocks (Supported in part by the National Science Foundation under Grant G2794.)

The various difference equations obtained from the integral form of the conservation equations in Eularian coordinates are being studied for their stability.

PART IV

GENERAL RESEARCH

Wave Function of the Hydrogen Molecule

The problem of obtaining the wave function of the hydrogen molecule (originally started at MURA by Nordsieck, Taub, Fosdick and Snyder) is being programmed for the IBM 704. This problem falls into three parts. First the two double equations for the hydrogen molecule ion are solved to obtain a set of basis functions. The first forty states will be used. These are formed into 114 normalized two-electron product basis wave functions. This portion of the programming is complete. In connection with it, it was necessary to program a routine which would obtain the intersection of the two eigenvalue curves given several points on each curve. Second, a matrix of the interelectron interaction energy is formed with these 114 wave functions as bases. Each matrix element is a 6-dimensional configuration integral which by analysis can be reduced to a 4-dimensional integral. This portion of the problem has been formulated and analyzed but not yet programmed. Two subroutines necessary for this routine are under preparation at MURA. Third, this matrix will be diagonalized to find the eigenvalues and eigenvectors which will in turn determine the hydrogen molecule wave function in terms of the two-electron basis functions. The appropriate matrix programs have been prepared at MURA.

PART V

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During October specifications were presented for 14 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1060. Numbers followed by T are for theses.

1060 Computer. Carry Propagation Studies. The problem is to study the probable characteristics of carry propagation for various types of logical design of adders. For some types of designs, the only reasonable way (at present) of estimating expected maximum carry propagation is by Monte Carlo methods which will be tried on Illiac. In other cases, recursive probability equations may be written which allow on easy direct calculation of probabilities.

1061 T Psychology. An Investigation of the Perceptual Space Concept. An investigation of the existence, reliability and validity of the "Perceptual Space Concept" will be carried out. "Perceptual Space" (SP) is a conception proposed by Cronback, who for several years has worked in the area of social perception. A perceiver rates, judges or perceives a given number of other persons, each on the same rating scale of adjectives, e.g., dependable, tense, passive. This abstractly defines the SP of the perceiver. Operationally, the responses to the items of the rating scale are factor-analyzed, yielding orthogonal dimensions. If he describes a number of other representative items, the position they occupy in this space indicates the perceiver's map or space of the interpersonal world. The central tendencies, variabilities and shape of the distributions is characteristic of this judge.

1062 T Sociology. Community-Library Relationships. The problem consists of 26 variables, about 1/2 of which are community figures, such as percent in the labor force, and 1/2 of which are library figures, such as per capita circulation. The problem is to find what, if any, relationship exists between these two sets of variables, and which of them are significant.

1063 Civil Engineering. Analysis of Simple Truss. The problem involves the computation of the stresses in each member of statically determinate bridge or building trusses. The program consists of a series of logical decisions to correlate the shape and makeup of the truss with the stresses in the members. This is followed by the evaluation of the expressions giving the stress in the members.

1064 T Chemistry. Solution of the Secular Equation for Molecular Vibrations. In the study of isotope effects in chemical reactions for molecules of most symmetry classes, the expression for the ratio of the rate constants can be reduced to a function solely of the normal modes of vibration of the reacting specie and the activated complex for both the normal molecules and their isotopically substituted counterparts. To calculate these normal modes, one will follow the so-called Wilson FG matrix method for which the secular equation can be represented as

$$\left| G - F^{-1}\lambda \right| = 0,$$

where G = kinetic energy matrix; F = potential energy matrix.

1065 Electrical Engineering. Non-linear Oscillation. This problem consists of solving a nonlinear differential equation which describes the flow of a viscous liquid in a tube. Such flows arise from consideration of acoustical problems involving second-order effects which are important at high-intensity levels. Although this differential equation can be solved by hand computing-machine operation for a short range of values of the parameters, it is not practical to solve this problem over a wide range of the values of the parameters by hand computing-machine methods. For numerical integration of the differential equation, $u' = \cos\theta - au^2$, a value of θ_o is chosen such that ua is assumed zero. The next zero of u is determined by a new θ_o and the integration is repeated until the periodicity is $180^\circ \pm .01^\circ$. The value of u is now printed as a function of θ.

1066 Psychology. A New Rotational Model for Factor Analysis. Schmid and Leiman (Psychometrika, 22:53-63, 1957) have developed a transformation which when applied to an oblique factor analysis solution in several orders, results in a single orthogonal rotated factor matrix. It is believed that the hierarchy of factors revealed by this transformation is particularly appropriate for most psychological

data. The purpose of this research is to use the technique in a series of problems which have been analyzed by other means and make a comparison of the results.

1067 Psychology. The Age Generality of Personality Factors Derived from Ratings, Questionnaires and Objective Tests. This study is designed to assess the generality of personality factors previously obtained in investigations of subjects at four different age levels (4, 6, 11 and young adult) by three different data-gathering procedures (rating, questionnaire, and objective test). Twelve sets of data are to be analyzed by correlating factor loadings on common marker variables within each medium across the various age levels for all possible pairs of studies.

1068 Sociology. Factors in Friendship and in Organizational Loyalties. Intensive interview and questionnaire data have been collected from 60 subjects in a prominent organization. The data include information on close friendships (numbers, dimensions, types) and on organizational activities, loyalties, and beliefs. The study hypothesizes a number of "friendship" factors (Problem 1), a number of "organizational loyalty" factors (Problem 2), and specific relations between these two sets of factors. These hypotheses will be tested.

1069 T Agricultural Economics. Comparison of Returns to Capital Between Areas of High and Low Soil Productivity. Two model farm situations have been selected: one on highly productive soils and one on soils of low productivity. A comparison will be made of the optional farm organizations with various amounts of capital available in each area. The method of linear programming will be used. The models employed will be dynamic in the sense that two production periods are being planned for each situation.

1070 T Psychology. The Perception of Self and Others by Normal and Hospitalized Subjects. One hundred and five normals and fifty-five mental patients were asked to rate themselves, a close friend, another close friend, a nonfriend, another nonfriend, others in general, and the ideal person. They used a rating scale consisting of 24 pairs of items (for example, one of the 24 pairs was: Friendly ____: ____: ____: ____: ____: ____: unfriendly). They also used the same type of scale, using different items, however, to rate themselves, others in general and the

ideal person. The first operation for which the Illiac is needed is to compute the relationship between each rating and every other one by using a "D" statistic. This consists of obtaining the difference (D) between any two ratings (self and other, for example) and then computing the square root of the sum, for the 24 items, of the D's squared. There are 21 $\sqrt{\Sigma D^2}$ that are to be computed for each person on the one scale and three on the other. The next operation for which the computer is to be used is to figure the intercorrelation among the 21 D's of the one scale and three of the other. This involves a total of 213 correlations.

1071 T Electrical Engineering. The Design of an Optimum Linear Coder and Decoder. Given the statistical power spectrum of the signal and the noise (noise power uncorrelated) to design the optimum linear coder and decoder so that the output will be the best rms approximation to the input or to the result of some linear operation on the input (such as the derivative of the input or prediction of the input). The problem is to be solved under the following restrictions: (1) The average signal power from the coder is prescribed. (2) The coder and decoder operators are linear and physically realizable (they are operators operating on the past and not on the future of the input). The method of solution is a modification of the standard methods of the calculus of variations (to take care of physical realizability) which leads to integral equations of the Wiener Hopf type. The solution of these equations for rational spectra leads to definite integrals (of the Poisson type).

1072 Structural Research. Calculation of Charts for the Rapid Evaluation of Structural Damage due to Atomic Blast Type Loadings. The program evaluates the peak pressure of an initially peaked, exponentially decaying force pulse which, acting on a single-degree-of-freedom system, will cause a given response of the system. The resistance is bi-linear. The program solves for the response at two given values of peak pressure and then interpolates for the desired response using Illiac Library Routine H-1. The response is obtained by Newmarks' β method of integration and the code for this is similar to that used in Problem Specifications 426, 439, and 630. The results of this research are presented in charts which make possible the rapid evaluation of structural damage due to atomic blast type loadings.

1073 Psychology. Personality Structure in Delinquent Males. A questionnaire of demonstrated effectiveness in differentiating delinquents from non-delinquents has been administered to 240 delinquent male subjects and to 240 matched non-delinquent subjects. Separate factor analyses of each set of data and a statistical match of the two resultant sets of factors is now required for determination of structural aspects of personality in the delinquent and non-delinquent youths.

Table I shows the distribution of machine time for the month of October.

Table I

	Hrs:Min
Regular Maintenance	36:00
Unscheduled Maintenance	8:26
Drum Engineering	44:53
R.A.R.	5:02
Leapfrog	46:42
Wasted	:00
<u>Use by Departments</u>	
Computer	16:02
Physics	27:47
Control Systems Lab.	109:24
Struct. Res.	116:24
Struct. Res. (AF 24994)	9:41
Psychology	34:40
Psychology (PH 1733)	5:54
College of Medicine	7:42
Electrical Engineering	3:31
Chemistry	21:28
Agriculture	16:32
Theor. and Appl. Mech. (ORD 593 IC)	:05
State Water Survey	10:33
Classes	13:28
Demonstrations	2:11
Miscellaneous	18:16
	556:13

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for October.

TABLE III

Reader Errors	1
Punch Errors	3
Scope Errors	4
Drum Errors	5
Control Errors	1
Unknown Errors	7
	21

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
10/1/57	20:00	:00	0		:00	:49	0
10/2/57	19:58	:02	2	(1) Drum failure (2) Unknown	:00	:50	0
10/3/57	18:37	1:32	2	(1) Unknown (2) Unknown	:00	:41	0
10/4/57	19:57	:03	3	(1) Unknown (2) Scope error Film jammed (3) Scope error Film jammed	:00	2:01	0
10/7/57	19:59	:01	1	(1) Scope error Film jammed	:00	3:04	0
10/8/57	20:00	:00	0		:00	:40	0
10/9/57	18:07	1:53	2	(1) R_3 push button bad, replaced (2) Unknown	:00	:56	0
10/10/57	19:59	:01	1	(1) Scope error Film jammed	:00	1:10	0
10/11/57	20:00	:00	0		:00	:47	0
10/14/57	20:00	:00	0		:00	1:20	0
10/15/57	19:20	:40	1	(1) Drum failure	:00	1:44	0
10/16/57	19:10	:50	1	(1) Reader error, wire broken to 1 hole "K"	:00	:46	0
10/17/57	19:59	:01	1	(1) Sprocket hole on tape not punched. Tape came from punch 4 on Illiac Punch Failure	:00	:56	0
10/18/57	19:42	:18	1	(1) Punch error, number 4	:00	1:05	0
10/21/57	20:00	:00	0		:00	1:02	0
10/22/57	20:00	:00	0		:00	1:23	0
10/23/57	20:00	:00	0		:00	:39	0
10/24/57	20:00	:00	0		:00	1:40	0
10/25/57	20:00	:00	0		:00	1:23	0
10/28/57	19:59	:01	1	(1) Unknown	:00	1:08	0

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
10/29/57	19:54	:06	1	(1) Drum failure	:00	1:05	0
10/30/57	19:57	:03	3	(1) Punch error Punch No. 4 (2) Unknown (3) Drum failure	:00	1:20	0
10/31/57	16:15	3:45	1	(1) Drum failure	:00	1:11	0
TOTALS	450:53	9:07	21		:00	29:00	0

Reports and Seminars

Seminars

"A Monte Carlo Program for Studying Crystal Statistics", by Dr. L. D. Fosdick, October 1, 1957.

"The Logical Organization of the New Computer", by Dr. D. B. Gillies, October 8, 1957.

"Statistical Study of a Switching Network", by Gene H. Golub, October 15, 1957.

"The Hydrogen Molecule (I)", by Dr. J. N. Snyder, October 22, 1957.

"Kinetic Theory of Gaseous Shock Waves", by Prof. A. T. Nordsieck, October 29, 1957.

Reports

Digital Computer Laboratory Report No. 80, "On the Design of a Very High-Speed Computer", October, 1957.

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UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

PART I: STUDY PROGRAM ON HIGH-SPEED COMPUTER

PART II: MATHEMATICAL METHODS

PART III: GENERAL RESEARCH

PART IV: ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

November, 1957

PART I

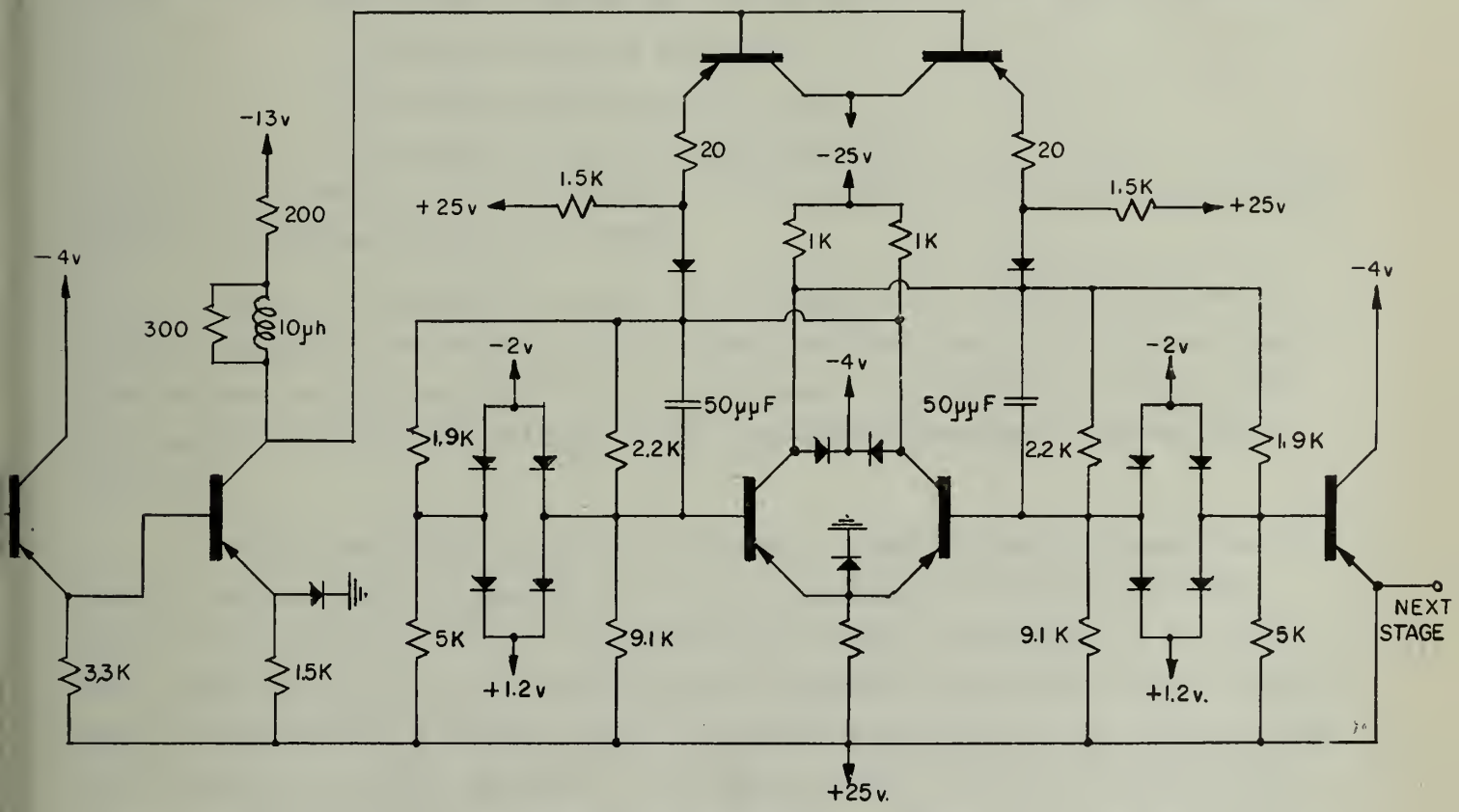
STUDY PROGRAM ON HIGH-SPEED COMPUTER

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition, this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. Basic Circuits

Using a slightly modified version of the standard Eccles-Jordan with GF-45011 transistors, a counter was designed which uses steering diodes to go into the collectors. The purpose of this was to obtain an independent estimate of the operation time of such a flipflop, the usual estimate being based on a racing register. It turned out that with speed-up capacitors and series-peaking in the driver preamplifier, frequencies of the order of 40 mc could be processed.



40 Megacycle Counter Stage

The above counter was duplicated to form a scale of four frequency divider to be used in synchronizing an oscilloscope with a low duty-cycle triggering device from racing registers.

A more elaborate synchronizing device for the 517 scope was also designed. The 21-transistor circuit (containing some simple logic and two Schmidt-Trigger flipflops) synchronizes the scope with selected cycles of a high repetition rate signal (from a racing register) whenever a low-frequency control signal comes along. Some dc-level problems were encountered and fixed and the unit provided good practice in assembling the basic circuits. The dc-level problem incidentally led to the re-examination of our last-moving-point design procedures which may have to be modified to take care of input signals which vary very slowly.

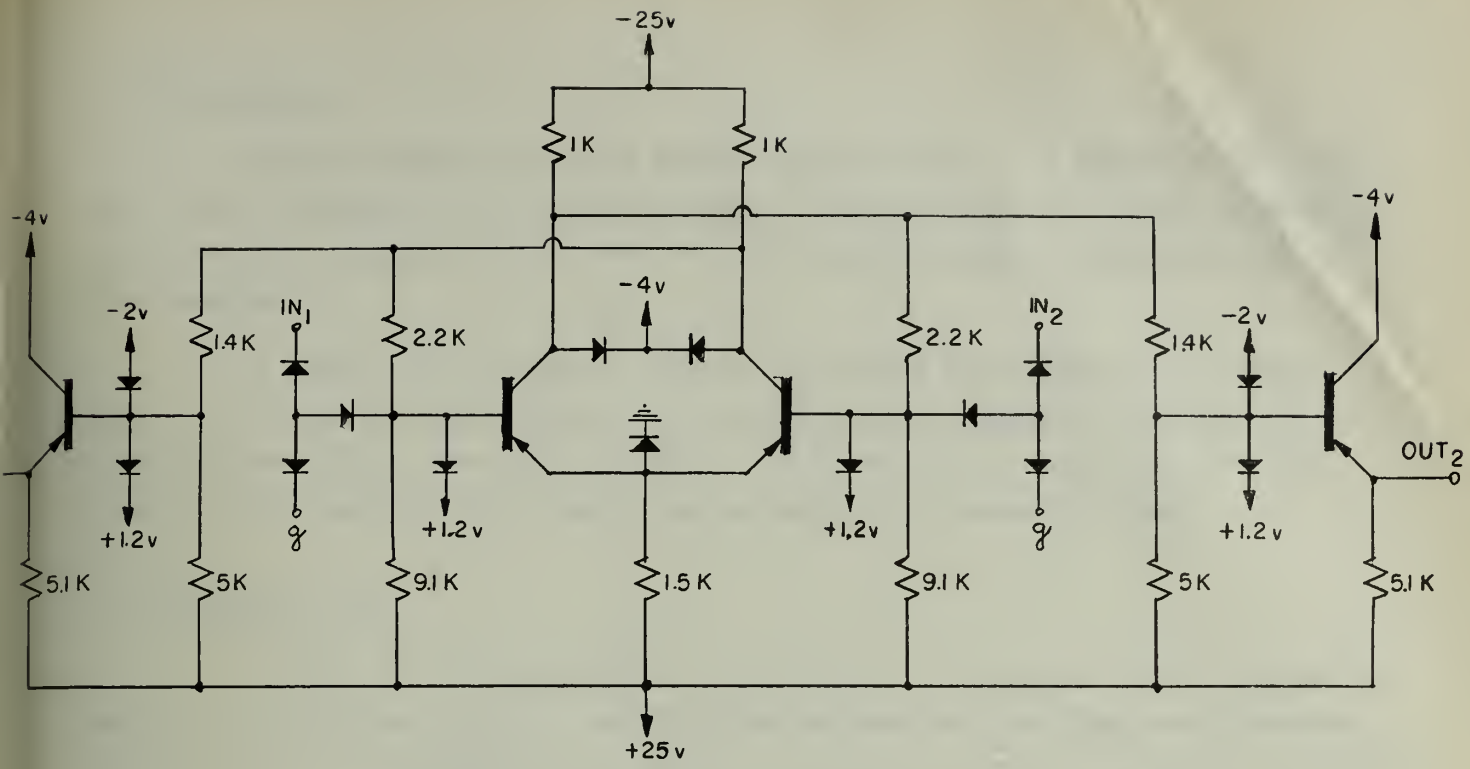
The building blocks shown in Chapter IV of Report 80 were modified as announced in the report for October. The new designs have the circuit values given in the following figures. Note that for these circuits

all transistors are WE GF-45011;
all diodes in collectors are NU T37D;
all other diodes are NU T37J;
all resistor tolerances are $\pm$ 2%;
all supply voltage tolerances are $\pm$ 3%.

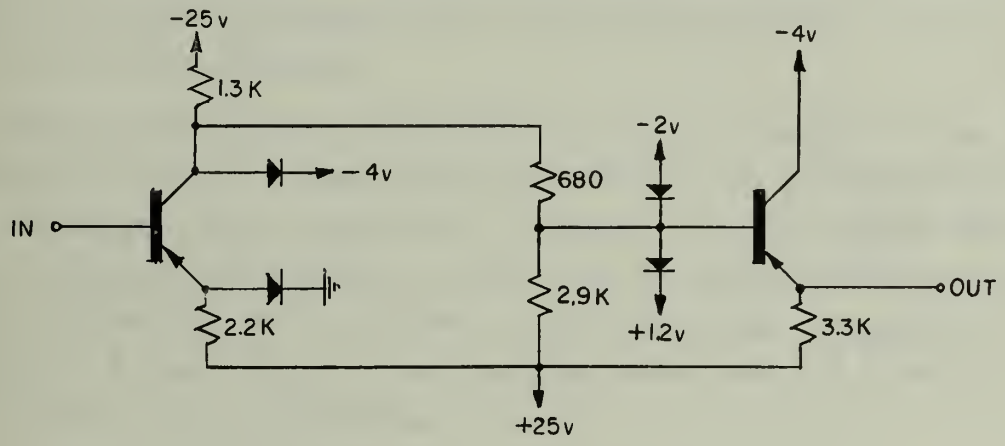
It should be remarked that the National Union diodes may be replaced by Qutronics Q5-250 ($\rightarrow$ T37J) and Q10-600 ($\rightarrow$ T37D).

The circuits shown on page 3 use bumping diodes in the collector to prevent saturation and diodes in the emitter and base leads to limit the reverse bias between emitter and base of the transistors. The nominal swing is $\pm$ 1.6v. The bumping voltages take account of the (average) emitter-base forward drop of 0.4v.

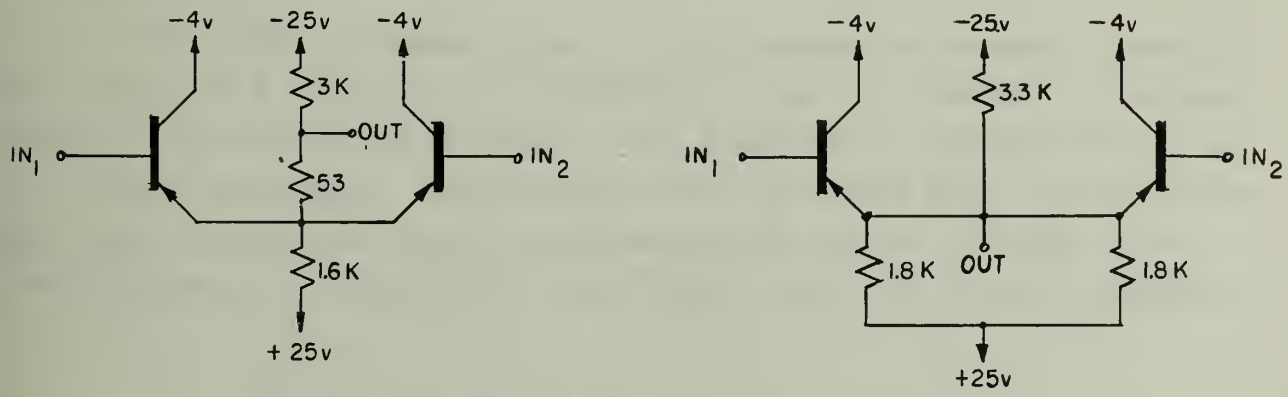
The flow-gating circuit (see October Technical Progress Report) was further analyzed and the general case ($\alpha \neq 1$, variable emitter-base forward drop) was calculated. The set of fundamental circuit inequalities $A > B > C \ldots$ etc., where $A(\ldots p_i \ldots)$, p_i being a general paramater (resistance value, α etc.) was transformed into a linear system by a Taylor Expansion and the linear system was solved by a relaxation method: This method gave the basic solutions to be tested by an analytical program. This analytical program is now in the early stages of preparation.



30 Millimicrosecond Eccles-Jordan Flipflop with Gates
(g = +1.2v → gate, g = -2v → non-gate)



15 Millimicrosecond NOT Circuit



5 Millimicrosecond AND and OR Circuits (Positive Logic)

2. Core Memory

Work was begun on a core memory read amplifier: A prototype was built and tested and appears to be satisfactory if the strobe pulse from the memory is short enough. Changes will be made as more specific memory characteristics become available.

A transistorized pulser capable of driving 50 μμf through 50 volts with a rise-time of less than 100 mμs was designed. Effects of transistor tolerance variations were investigated. The pulser would, when used with one stage of high current vacuum tubes, be suitable for a current driver.

3. Arithmetic Unit

A class of division methods, believed to be new, was devised during the month. For arbitrary radix r, the division methods are such that each quotient digit is one of the integers -n, -(n-1), ..., -1, 0, 1, 2, ..., n where n satisfies $\frac{r-1}{2} \leq n \leq r-1$. The method can be contrasted with conventional non-restoring division, for which each quotient digit is one of the integers -(r-1), ..., -1, 1, 2, ..., r-1, with 0 excluded.

For the new computer, the choice n = 2, r = 4, leads to a new base 4 division method which is in some sense the inverse of the multiplication method described in Chapter VIII of Report 80. The base 4 division method shares the conditional complementing-doubling circuits with the multiplication, and does not require the tripling of the divisor to full precision. Circuits to compare on the order of 8 binary digits of partial remainders with 1/2 y and 3/2 y are required, where y is the standardized divisor.

4. Control Studies

The portion of Monte Crysto I which computes the change in energy of the system when a pair of atoms are interchanged has been recoded for the new computer. This portion of the Monte Crysto I program is the major part of the main loop of the program. Estimating the time to execute other portions of the main loop, assuming that they too were recoded for the new computer, it was found that one pass through a 4000-atom lattice would take about 2.4 seconds on

the new computer# compared with 60 seconds for the same calculation on the IBM 704; i.e. the program would run about 25 times faster on the new computer. Estimates were made conservatively so the ratio 25 should represent a lower bound. It was found that the running time of the program was controlled by the memory access time. There was virtually no overlap in the operation of the arithmetic control and memory access. It was also found that there was very little opportunity to effectively use the short loop feature. The loops generally required more than the 8 control groups allowed in the short loop.

In writing this program it would have been convenient to have had available the instructions: b' = 0 (short); b' = b + m (long); a' = a and m (long or short). The latter instruction is convenient because it is frequently desired to test the result of an AND instruction for zero.

During this period a fairly simple-minded criterion for answering in an approximate way the question of whether the memory access time or the arithmetic operation time governs the overall operation time of a sequence of instructions was applied to the data presented in File No. 224 "A Study of the Order Types and References to Store in some Illiac and Ferut Library Routines" by J. H. Chung, C. C. Gotlieb and D. E. Muller. We define a unit arithmetic operation as a hypothetical operation requiring for its execution a time equal to an addition time. Thus, in terms of execution time a multiply instruction is equivalent to ten unit arithmetic operations in the new computer; a shift of one place is equivalent to 1/4 of a unit arithmetic operation time (shift time $\approx$ .08 μs in the new computer). We define, for a sequence of instructions,

n_1 = average number of data requests per unit arithmetic operation,

n_2 = average number of data writes per unit arithmetic operation,

n_3 = average number of instructions obeyed per unit arithmetic operation,

p_1 = number of words of data read per memory access,

The number of divide instructions is negligible, For the other operations the following times were assumed: multiply, 3.5 μs; all instructions exclusive of multiply and divide, .35 μs; memory access time, 1.5 μs.

p_2 = number of words of data written per memory access,

p_3 = number of instructions read per memory access for instructions,

λ = ratio of memory access time to unit operation time,

$$s = \lambda\left(\frac{n_1}{p_1} + \frac{n_2}{p_2} + \frac{n_3}{p_3}\right) .$$

If the execution time for the sequence of instructions is to be governed by the arithmetic speed rather than the memory access time then

$$s < 1 .$$

This is just a way of expressing the condition that the average memory access time must be less than the average arithmetic operation time. It is assumed in the above that there exists a "very" high-speed auxiliary storage with capacity sufficiently large to hold words read in blocks, as determined by the p's, from the conventional memory.

The quantities n_1, n_2, n_3 have been computed from the data of File No. 224 (Table 1a) and are shown in the table below. Using $p_1 = p_2 = 1$, $p_3 = 3$ and $\lambda = 5$, assuming them to be representative for the new computer, the quantity s has been computed and is also shown.

	n_1	n_2	n_3	s
Runge-Kutta (50 steps on J_o)	0.351	0.224	0.660	3.98
Polynomial Root (12 roots)	0.281	0.193	0.692	3.52
DOI	0.384	0.212	0.851	4.40
L-2 (12 equations without input)	0.280	0.175	0.550	3.19
Eigenvalue (without input)	0.283	0.145	0.523	3.01
Circuit Analyzer	0.478	0.261	1.02	5.40

These statistics have also been obtained for an analysis of variance program used by the Agronomy Department.

	n_1	n_2	n_3	s
Analysis of Variance	0.824	0.104	0.380	5.27

In every case $s > 1$[#], thus indicating that the execution time is controlled by the memory access time. This analysis neglects the advantage to be gained from using the two fast access registers in the new computer for temporary storage. Proper account of this would reduce n_1, probably not by more than 1/2. However, it is obvious from the above statistics that such a reduction in n_1 will not give $s < 1$ - even with $n_1 = 0$, s is > 1 in every case. This analysis also neglects the advantage to be gained from using short loops with the control groups in O_1 and O_2. Proper account of this would reduce n_3. It is unlikely that the reduction would amount to as much as 1/2 but even assuming this favorable estimate, and reducing n_1 by 1/2 we still obtain $s > 1$ in every case. It should be recognized that this problem is not obviated by advanced control alone. What is necessary is a decrease in λ or an increase in the values of the p's, or both in appropriate combination.

Assuming that λ is as small as possible let us see how large the p's must be to satisfy $s < 1$. Take $p_1 = 6$, $p_2 = 6$, $p_3 = 12$, then we note that in the worst case, the circuit analyzer, this is just sufficient to make $s \approx 1$ taking n_1, n_2 and n_3 directly as given above. If we reduce n_1, n_2 and n_3 each by 1/2, then $p_1 = 3$, $p_2 = 3$, $p_3 = 6$ give $s \approx 1$. These two sets of values represent upper and lower limits on the p's. If we compromise on $p_1 = 4$, $p_2 = 4$, $p_3 = 8$ we require a 4 word block read and write for data and an 8 word transfer for instructions. This is just the proposal in the appendix to Chapter 3 of Report 80. The above arguments seem to favor strongly such a scheme over the one proposed in the main body of Chapter 3.

[#] Note that the "Data Analysis" programs have the largest s.

PART II

MATHEMATICAL METHODS

1. Iterative Methods for Solving Systems of Linear Equations (Supported in part by the Office of Naval Research under Contract N6ori-07130.)

It has been shown by von Neumann that a class of iterative methods for solving the system of linear equations

$$Ax = y$$

may be described by the equations

$$x_{i+1} = Gx_i + Hy$$

where the matrices G, H and A are related by the equation

$$G + HA = 1,$$

and H is a non-singular matrix. It then follows that

$$x_{i+1} - x = G(x_i - x)$$

$$x_{i+1} - x_i = G(x_i - x_{i-1})$$

$$H(y - Ax_{i+1}) = GH(y - Ax_i) .$$

The averaging of a collection of iterates has also been considered by von Neumann.

A program has been initiated to study by numerical and analytic means the effect of making various choices for the coefficients of the matrix H given above in terms of the coefficients of the given matrix A. Once H is determined G is known. The criteria for choosing H are (1) that the computing algorithm be simple, and (2) that the convergence, as measured by the behavior of the norm of residuals (the difference of successive iterates or the difference between an iterate and the true solution) be as rapid as possible. In view of the relations given above this implies that the proper values of the matrix G be kept as small as possible in absolute value.

The study includes considering the question as to whether an averaging of a number of iterates leads to closer approximations to the solutions.

2. Minimization of Functions of Several Variables

1. In connection with the problem of reducing interferometer data from earth satellites, a new and very promising method of minimizing a function of n variables has been found. If F is the function, with suitable continuity and differentiability conditions, then the extrema in the interior of the region of definition are those points $\{\underline{x}\}$ for which $\frac{\partial F}{\partial x_i} = 0$, $i = 1, 2, \ldots, n$. Such extrema can be minima, maxima or saddle points. If the point $\underline{a}$ is sufficiently close to a minimum, the system of equations

$$\frac{\partial F}{\partial a_i} + \frac{1}{2!} \sum h_j \frac{\partial^2 F}{\partial a_i \, \partial a_j} = 0$$

can be solved for $\underline{h}$, provided $\left\| \frac{\partial^2 F}{\partial a_i \partial a_j} \right\|$ is not singular, and $\underline{a} + \underline{h}$ is a better approximation to the minimum. This is the Newton-Raphson method in n-dimensions, and requires estimates of the first and second derivatives, obtained, in general, from numerical differentiation.

The method actually used consists of estimating the above partial derivatives by central difference methods, and using the above equations to obtain numbers proportional to $\{h_i\}$, and then performing a walk in that direction (positive or negative) in which F decreases. When the function fails to decrease, quadratic interpolation is used to obtain the minimum in that direction. Partial derivatives are then re-evaluated and the process repeated.

If all partial derivatives are $O(1)$[#] and the round-off error in calculating F is $O(2^{-39})$, then the step interval for computing first derivatives is $O(2^{-13})$ and the error in estimating first derivatives is $O(2^{-26})$, whereas the optimum step interval for calculating second derivatives is $O(2^{-20})$. By making the process repetitive, the absolute error in the location of the minimum is $O(2^{-26})$.

The effect of introducing the walk is first of all to carry the operating point away from a maximum or saddle point if it happened to be near one; and secondly to make the distance travelled not depend on an extrapolation from local information. As the operating point approaches the minimum, and the second partial derivatives approach their limiting values, the method resembles the iterative

[#] O = "of the order of"

solution to a set of linear equations for which an extrapolation factor is calculated in such a way that the next walk will be in a direction orthogonal to this one. Finally, as the operating point gets very near the true minimum, the extrapolation factor tends to 1 (no extrapolation).

The accuracy of the method depends only on how accurately the first derivative can be estimated by finite difference methods. If unknown derivatives are assumed to be O(1) then the following table applies:

Formula for first derivative	Optimum step interval h	Absolute error
2 point	$\approx 2^{-13}$	$\approx 2^{-26}$
4 point	$\approx 2^{-9}$	$\approx 2^{-31}$

For the 4 point formula, points should be chosen at $x_i \pm h$ and $x_i \pm \frac{1}{2}(3 + \sqrt{5})h$. However, numerical differentiation of unknown functions is a very risky business, especially with large step intervals. One advantage of the method described is that it does not depend, for its accuracy, on a very accurate estimate of second derivatives.

2. A method applicable to evaluating determinants, solving linear algebraic equations, inverting matrices, and determining characteristic equations without round-off error, is being tested. The problem is first scaled so every coefficient is an integer. Then integer multiples of one row are subtracted from another in systematic fashion. This will be described for triangularizing the matrix $\|a_{ij}\|$. The elements of the first column $\{a_{i1}\}$ are first ordered in absolute value. Suppose a_{i1} is the largest and a_{j1} is the second largest. If k is the integer for which $k|a_{j1}| \leq |a_{i1}| < (k + 1)|a_{j1}|$ then a multiple $\pm k$ of the jth row is added to the ith row. This decreases the absolute value of the leading coefficient of the ith row to less than $|a_{j1}|$, and it remains an integer. This process is repeated until all but one of the leading coefficients of the rows are zero, the remaining one being the highest common factor of the original leading coefficients. The process is then repeated on the second column of all rows except that which ended with a non-zero leading coefficient in the first row. Continuing in this way, the matrix is eventually triangularized. The calculation requires multiple precision integer arithmetic,

however numbers do not grow as fast as might be expected. The total number of single-length additions required to triangularize an n x n matrix appears, experimentally, to be less than

$$n^3 \sqrt{n} \; \frac{d}{2}$$

when d is the average number of decimal digits in the original coefficients.

PART III

GENERAL RESEARCH

Satellite Data Reduction

An attempt is being made to analyze the radio interferometer data taken from the Russian satellites. These programs are also being prepared so that observations on forthcoming U. S. satellites can also be treated. An expected theoretical antenna pattern can be determined as a function of the distance, height, time and orbit inclination of the satellite at closest approach to the observing station. This is then compared to the observed antenna pattern and the weighted discrepancies minimized as a function of the four variables.

It is hoped that information on the refracting properties of the ionosphere can be extracted from these discrepancies. Several working programs have been produced.

The program discussed above exploits the very powerful technique of problem-solving by numerical minimization of an appropriately defined function with respect to its variables. This laboratory has used a series of routines (H-3, H-4, H-5, H-6) for this purpose which predominantly make use of gradient methods. The efficient minimization of a general function is a difficult task which can frustrate practically any method. Experience with the problem substantiate this. It is therefore felt that more efficient methods of function minimization should be investigated. This is especially true in the light of the new computer since more complicated functions of a greater number of variables will certainly need to be treated. (See section 2 under Mathematical Methods of this report.) The function occurring in connection with the satellite problem is sufficiently complicated that it yields an excellent non-trivial test case to which to apply potentially efficient methods. In fact, two methods (in addition to the gradient method) have been tried with some success.

PART IV

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During November specifications were presented for 10 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1074. Numbers followed by T are for theses.

1074 Computer. DM-Satellite Data Reduction. Given the times at which a satellite crosses the various lobes of two antenna arrays, a distance of closest approach to the observing station and the time of this approach are chosen so as to be most consistent with the given data.

1075 Education. Language Test Revision. The major factors contributing to total variance are to be found in a revised and restandardized language test.

1076 Enrico Fermi Institute for Nuclear Studies. Geomagnetic-Geographic Coordinate Transformation. The transformation of geographic to geomagnetic coordinates is necessary so that a ship bearing a standard University of Chicago - IGY neutron pile may follow constant geomagnetic latitude and longitude courses on a trip to and from Antarctica. The purpose of this trip is twofold: 1) to plot the intensity of cosmic rays as a function of the position on the earth's surface and 2) to observe time variations in cosmic ray intensity in such a manner that the observations obtained on the ship may be easily correlated with those at permanent stations.

1077 Computer. Library Program for Matrix Multiplication Which Uses the Drum. A revised matrix multiplication program is to be prepared for the library.

1078 T Chemical Engineering. Effect of Heat Transfer upon Flow Field at Low Reynolds Numbers. The problem is to predict the temperature and velocity fields in a fluid as it flows at a low Reynolds Number in a vertical tube with

a constant wall temperature. The fluid enters the heated section with a fully developed laminar velocity profile and at a uniform temperature.

Since the non-linear hydrodynamic differential equations cannot be easily solved, an approximate method suggested by Lighthill and modified by this work is being attempted. This method leads to four simultaneous linear first-order differential equations with four parameters to which a numerical solution is sought.

Since it is not known what sort of numbers will be involved, floating decimal routines will be used throughout.

1079 Physics. π^0 Photoproduction from Hydrogen. The problem is to calculate the counter efficiencies for the photoproduction of π^0 mesons from hydrogen. The dynamics of the process, the energy loss of the recoil protons in the target, and the geometry of the counters must be included.

1080 T Mining and Metallurgical Engineering. 3-Dimensional Network Models of Porous Media. The porosity is to be found as a tabulated function of the pore size distribution and a quantity which relates the length of a pore to its radius.

1081 Institute of Communications Research. Emotional Factors in Attitude Change. A statistical study is to be made of the relationships between personality dimensions, mood changes, and attitude changes produced by four different mass communications. Audience responses were obtained for 52 variables, over a period of 8 weeks.

1082 Psychology. Pattern Analysis by Q-Technique. This problem is a preliminary investigation of the application of Q-technique in factor analysis to pattern analysis. The data used would be clinical and psychometric. The programs to be used would be drawn from the Social Sciences Library.

1083 Computer. Floating Precision Linear Equation Solver. Linear algebraic equations can be considered, after appropriate scaling, to have integer coefficients and integer right-hand sides. The matrix is first triangularized

by, in principle, a highest common factor process on the current left-hand column. That is, in general, an integer multiple of the row whose left-hand coefficient is second largest is added/subtracted to/from the equation whose left-hand coefficient is largest. This process is continued until all but one equation have zero coefficients. The resulting system has its order reduced by one and the process is repeated. Back substitution is done in the usual way for rational fractions. The resulting program can, of course, be used for evaluating determinants, inverting matrices, and obtaining characteristic polynomials, exactly.

Table I shows the distribution of machine time for the month of November.

Table I

	Hrs:Min
Regular Maintenance	22:24
Unscheduled Maintenance	1:13
Drum Engineering	36:46
R.A.R.	5:04
Leapfrog	31:43
Wasted	:00
<u>Use by Departments</u>	
Computer	39:47
Physics	20:14
Control Systems Lab.	90:06
Structural Research	86:09
Struct. Res. (AF 24994)	35:24
Psychology	24:58
Electrical Engineering	2:51
Chemistry	29:43
Agriculture	16:27
Theor. and Appl. Mech. (ORD 593 IC)	:20
Inst. of Comm. Res.	4:39
State Water Survey	7:40
University of Chicago	1:11
U. S. Navy	:34
Classes	28:24
Demonstrations	3:03
Miscellaneous	10:43
	499:23

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for November.

TABLE III

Memory Errors	1
Reader Errors	2
Drum Failures	2
Punch Errors	0
Control Errors	0
Unknown	3
	8

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
11/1/57	20:00	:00	0		:00	:44	0
11/4/57	20:00	:00	0		:00	:41	0
11/5/47	20:00	:00	0		:00	:52	0
11/6/57	20:00	:00	0		:00	:42	0
11/7/57	20:00	:00	0		:00	:51	0
11/8/57	20:00	:00	0		:00	:50	0
11/11/57	19:31	:29	2	(1) Memory Error fuse to address generator blew. Memory pos 2^{-20} bad (2) Unknown			
11/12/57	19:47	:13	2	(1) Reader "F" error (2) Reader "F" error	:00	:45	0
11/13/57	20:00	:00	0		:00	:50	0
11/14/57	20:00	:00	0		:00	:40	0
11/15/57	20:00	:00	0		:00	:42	0
11/18/57	20:00	:00	0		:00	:50	0
11/19/57	20:00	:00	0		:00	:40	0
11/20/57	20:00	:00	0		:00	:42	0
11/21/57	19:40	:00	0		:20	:43	0
11/22/57	20:00	:00	0		:00	:39	0
11/25/57	20:00	:00	0		:00	:41	0
11/26/57	19:58	:02	2	(1) Unknown (2) Unknown	:00	:37	0
11/27/57	18:07	1:53	1	(1) Drum failure	:00	:20	0
11/29/57	19:38	:22	1	(1) Drum failure	:00	:43	0
TOTALS	396:41	2:59	8		:20	15:02	0

Reports and Seminars

Seminars

"The Hydrogen Molecule (II)", by Dr. J. N. Snyder, November 5, 1957.

"Some New Techniques in Logical Design", by Dr. D. E. Muller, November 12, 1957.

"A Study of Parallel One's Complement Arithmetic Units with Separate Carry or Borrow Storage", by Gernot Metze, November 26, 1957.

Reports

Digital Computer Laboratory Report No. 81, "Parallel One's Complement Arithmetic Units with Separate Carry or Borrow Storage", November 11, 1957.

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DIGITAL COMPUTER

UNIVERSITY OF ILLINOIS

FINANCIAL REPORT

NOVEMBER 30, 1957

	DIGITAL COMPUTER	U. S. A.E.C.415	DIGITAL COMPUTER IND.COST	SOC.SCIENCE RES.COUNCIL	COMPUTER SERVICE	NATIONAL SCIENCE FOUNDATION	U.S. NAVY TASK 15	U.S. NAVY TASK 30	TOTAL
Free Balance	7,350.21 [1]	9,011.18 [2]	2,061.85	700.00	45,318.40	24,315.30 [3]	27,918.69 [4]	13,529.59 [5]	130,205.22
Equipment	4,585.93				50,026.19				54,612.12
Materials	2,125.50	32,050.13			100,939.37	334.93	23.52	78.45	135,551.90
Sal./Wages	47,431.28	39,234.00			174,354.28	6,310.81	1,150.00	61,732.47	330,212.84
Overhead		14,612.76				1,038.47	428.38	23,835.86	39,915.47
Workmens Comp.		784.68				95.42	22.99	1,229.68	2,132.77
Retirement		861.13			163.20	18.07			1,042.40
Travel	281.40	2,350.26			2,084.89	165.95		1,565.90	6,448.40
Tele./Teleg.	938.45	1,095.86			1,824.12	21.05		72.65	3,952.13
Building					365.78				365.78
Totals	55,362.56	90,988.82			329,757.83	7,984.70	1,624.89	88,515.01	574,233.81
					Funds Expended - Previous Allowances.				1,071,907.34
					Total Expenditures, 2/1/49 to date.				1,646,141.15

1. Through June 30, 1958 (Exp./Wages)
2. Through November 30, 1957
3. Through August 31, 1958
4. Through October 31, 1958
5. Through June 15, 1958

UNIVERSITY OF ILLINOIS

GRADUATE COLLEGE

DIGITAL COMPUTER LABORATORY

TECHNICAL PROGRESS REPORT

Teaching and graduate research are not, in general, reported herein.

PART I: HIGH-SPEED COMPUTER PROGRAM

PART II: SWITCHING CIRCUIT THEORY

PART III: MATHEMATICAL METHODS

PART IV: GENERAL RESEARCH

PART V: ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

December, 1957

PART I

HIGH-SPEED COMPUTER PROGRAM

This work is supported in part through Contract No. AT(11-1)-415 of the Atomic Energy Commission. The contract is supported jointly by the Atomic Energy Commission and the Office of Naval Research. In addition, this work is supported through Contracts N6ori-07130 and Nonr-1834(15), both from the Office of Naval Research.

The University of Toronto is participating in this work through staff members of its Computation Centre.

1. Transistor Circuits

In order to compare the speeds of circuits wired in bread-board fashion and plug-in units, the operation times of two racing registers using the Eccles-Jordan flipflops given in the November Report were measured. For a four flipflop register the times for both were 28 ± 2 mμs/operation; the plug-in units having a slight edge. It should be mentioned, however, that by varying the supply voltages by the allowed amount (± 3%) the operation times can change by as much as 10%.

A 4-digit shifting register was built using 8 of the above mentioned plug-in units. Experiments with a four-phase logical oscillator of the type used in Illiac (two phases of which controlled the drivers for the up-gates and the down-gates) showed that the transmission of information takes less than 100 mμs. This encouraged us to design a two-phase logical oscillator and improve the drivers according to Figure 1 and Figure 2. In this fashion, gate-pulses of less than 50 mμs length were obtained and error-free shifting was observed for many hours. A life test will be started soon. Figure 3 shows some timing diagrams.

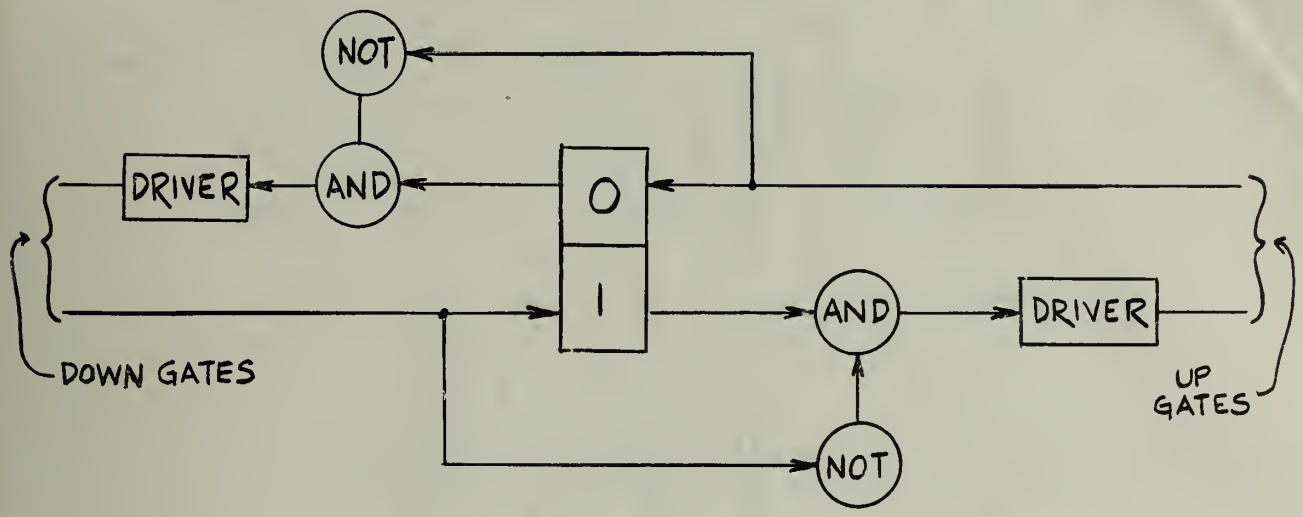

Figure 1

50-mμs Logical Oscillator
(circuit values of FF, AND and NOT--see November report)

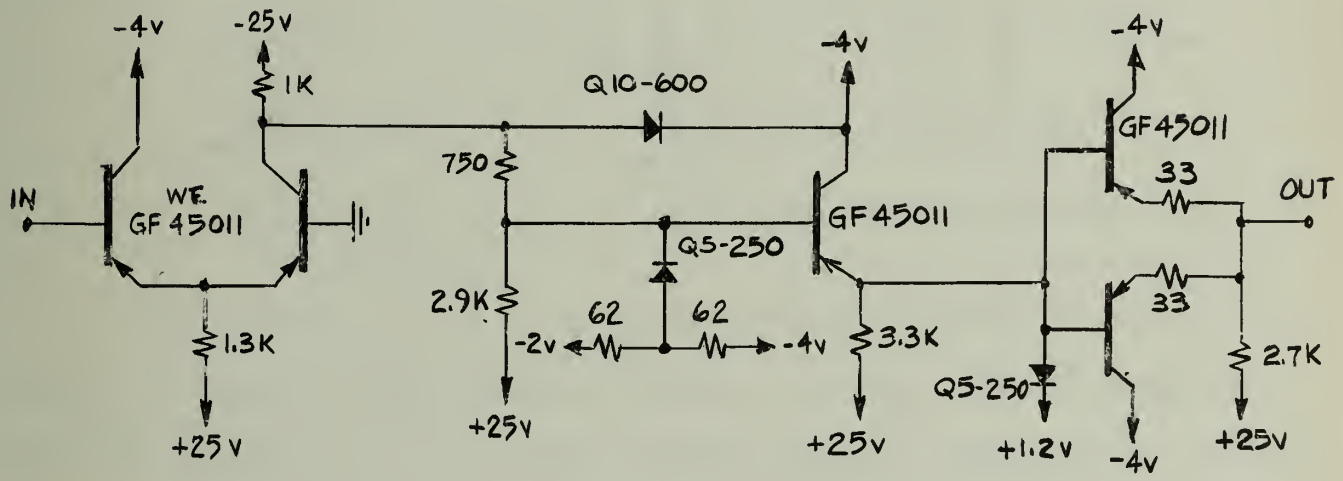

Figure 2

50-mμs Driver

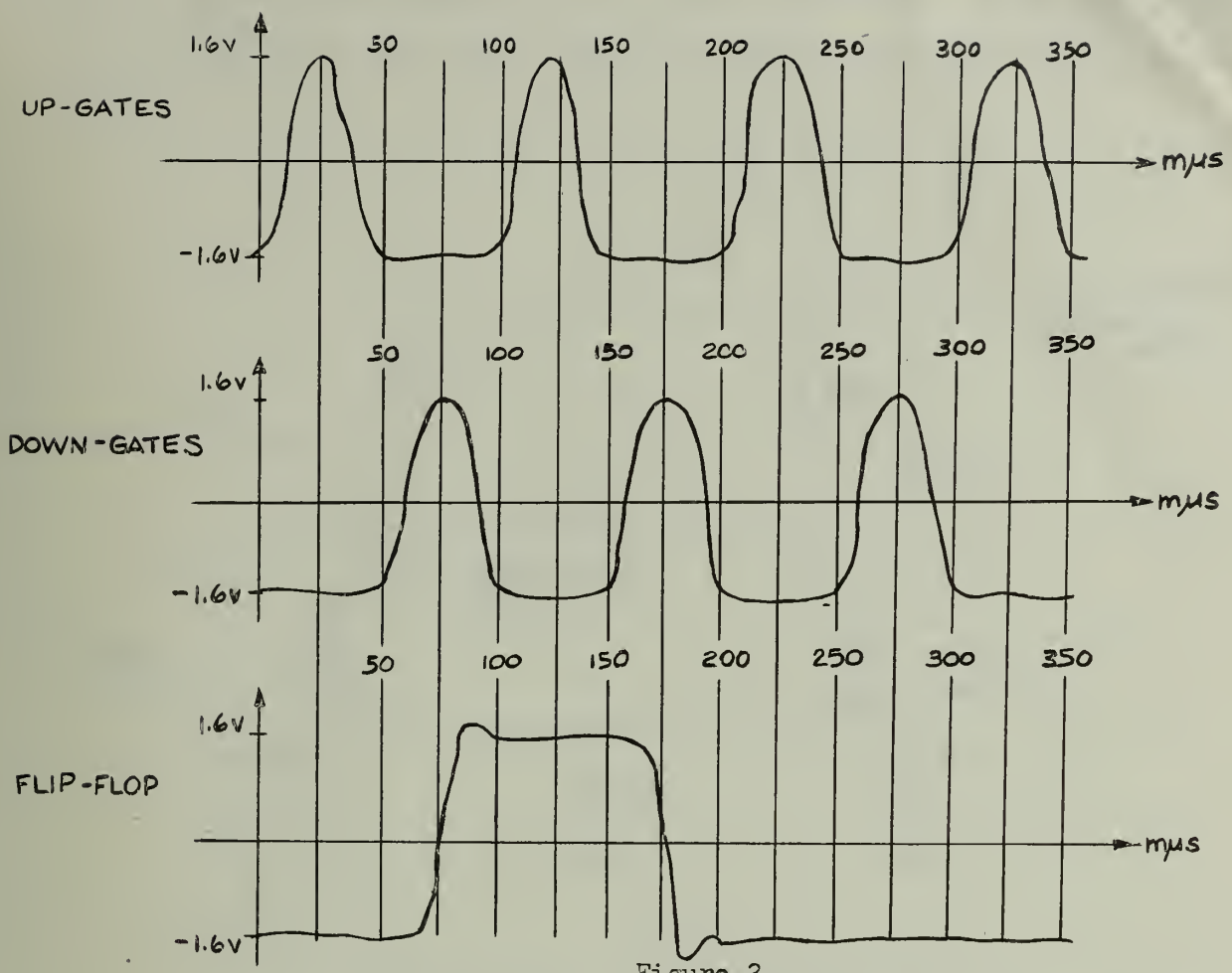

Figure 3

Timing Diagram for the 50 mμs Shifting Register--Pattern 0001.

The methods indicated in the November Report have resulted in the design of a flow-gating flipflop which satisfies our usual tolerance conditions (2% resistors, 3% power supplies) with the difference that transistors must have $\alpha > .98$ instead of the usual $\alpha > .95$. The analytical program mentioned last month is now completed and has been used to check the flow-gating flipflop circuit values. This program calculates the voltages and currents under the "worst case" conditions. The input values are the nominal values of resistors,

power-supply voltages, alphas, diode and base-emitter drops as a function of current and finally the tolerances on all these parameters. The circuit values are given in Figure 4. Note that a bumping diode has been added in the output collector.

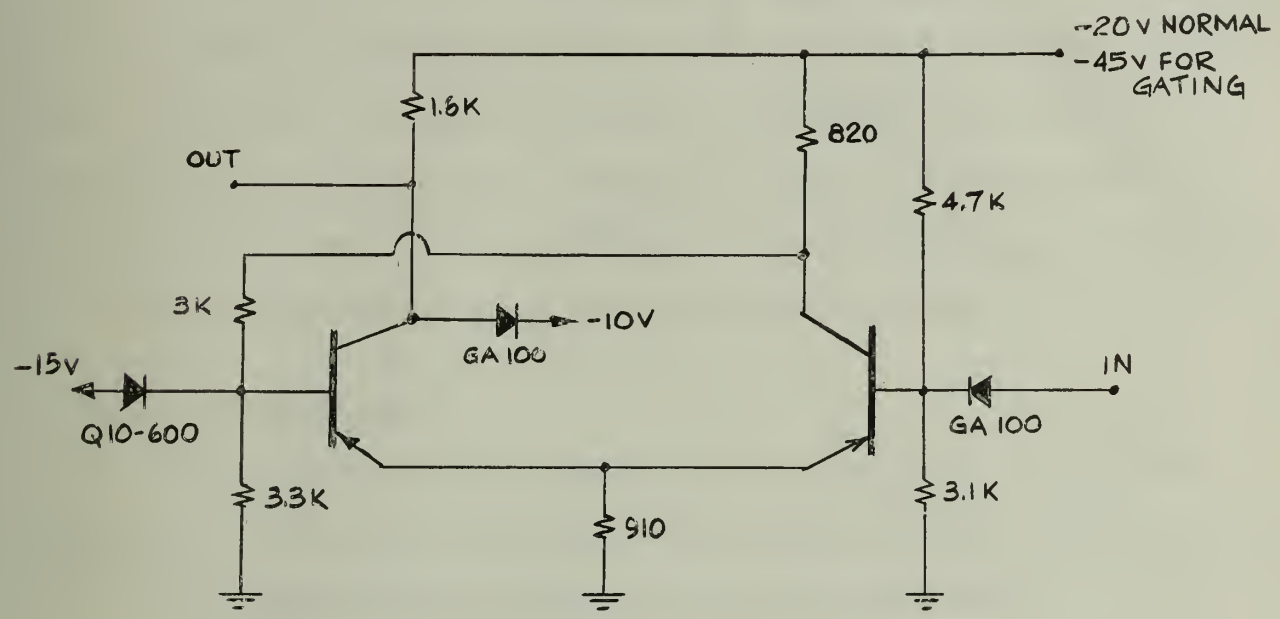

Figure 4

Circuit Values for a Flow-Gating Flipflop
(resistor tolerances ± 2%, power supply tolerances ± 3%, $\alpha > 0.98$)

2. Control Studies

Storage Requirement Studies

A study has been made of the problem of solving a three-dimensional hyperbolic differential equation (one time variable) by finite difference means on the new proposed computer. This problem makes severe demands on the core memory, drum, and magnetic tapes, since a very large amount of temporary storage

is required. The problem is to rearrange the order of calculation so as to advance the time variable by a number of step intervals for each pass of the data and to store large numbers of data on the drum, to be used frequently, and a smaller amount in the core memory, to be used even more frequently.

For a given size of drum memory and core memory, and given speeds for reading data to and from the drum and magnetic tapes, a system of 5 inequalities must be satisfied in order that the memory time not exceed the time for calculation. The parameter in those equalities is the number of mesh points in any one dimension. By allowing other quantities to vary, this can be used to obtain estimates (at least for this problem) of the relative sizes of the memories and the way in which magnetic tape speeds influence these sizes.

Floating Point Studies

Three versions of the 1.7 precision floating binary interpretive routine (69-bit fractional part and 10-bit exponent) have been used. These are:

(a) Standardize the accumulator after every arithmetic operation.

(b) Standardize the accumulator only before storing its contents, or if it would otherwise overflow.

(c) A modification of the Metropolis system of significance indicated by leading zeros or leading ones, in which a product is shifted left one place, if this does not cause overflow, and a quotient has the same number of significant bits as the least significant of the divisor and dividend.

Preliminary experiments indicated that (a) was not detectably better than (b), and since it requires more complex circuitry and is slower, it was not extensively tested.

The floating binary experimental routines were used during the month on two classes of problems--matrix inversion by the elimination method, and proper values of symmetric matrices by Givens method.

The matrices inverted so far have been:

(a) Hilbert matrices $\|a_{ij}\|$ when $a_{ij} = \frac{1}{1+j-1}$, $i, j = 1, 2, \ldots, n$,

for $n = 3, \ldots, 15$ for standardize on store

and $n = 3, \ldots, 13$ for modified Metropolis

(b) Power matrices $a_{ij} = i^j$, $i = 1, 2, \ldots, n$

$j = 0, 1, \ldots, n - 1$

for $n = 3, \ldots, 15$ by both methods

These matrices have inverses which can be computed directly (for the inverse of the Hilbert matrix see the NBS monograph on Matrices and Linear Equations). For the power matrix, the inverse may be found as follows:

Let $\|b_{ij}\|$ be the adjoint matrix.

Then $\sum i^j b_{jk} = 0$ when $i \neq k$.

Hence b_{jk}, for fixed k, are the coefficients of the polynomial of degree $n - 1$ where zeros are $1, 2, \ldots, k - 1, k + 1, \ldots, n$. The inverses of both classes of matrices consist entirely of non-zero elements.

If c^*_{ij} is an element in the exact inverse, and c_{ij} is its computed approximation, then the relative error γ_{ij} is defined by

$$\gamma_{ij} = \frac{c_{ij} - c^*_{ij}}{c^*_{ij}} .$$

The following measures of error have been computed for the above matrices:

$$\frac{1}{n^2}\sum|\gamma_{ij}| \ ,$$

$$\sqrt{\frac{1}{n^2}\sum\gamma_{ij}^2} \ ,$$

$$\max_{i,j}|\gamma_{ij}| \ ,$$

$$\frac{1}{n^2}\sum\gamma_{ij}.$$

The errors have not yet been analyzed.

As a further test of methods for floating point arithmetic and to relate loss of precision during matrix inversion to the ratio of the largest to smallest proper value, Givens method has been used to obtain proper values of both the Hilbert matrices and the inverse of the Hilbert matrices of orders 3 through 13. As n tends toward infinity, the ratio of the largest to smallest proper values for the Hilbert matrix tends toward e^{-3n}, so numerical inversion rapidly becomes inaccurate as n increases.

PART II

SWITCHING CIRCUIT THEORY

(This work is supported in part by the Office of Naval Research under Contract N6ori-07130.)

1. Combinational Circuits

A study was made of combinational switching circuits formed from AND, OR, and NOT elements. A method was found for generating a combinational circuit yielding a given set of switching functions which contains no more NOT elements than any other combinational circuit producing the same switching functions. It was also shown that no circuit having n inputs requires more than k NOT elements, where k = the least integer no smaller than $\log_2 (n+1)$. A 2^r-1 digit adder having r NOT elements has been designed by this method, and has been proved to have a minimum number of NOT elements.

2. Distributive Circuits

Several new results have been obtained in the theory of distributive circuits having cyclic behavior. A theorem stronger than (8:D) of Report 78 was found to apply to distributive circuits. The stronger theorem states that in a circuit which is distributive with respect to some initial state u if A and B are two equivalence classes of states such that $A \mathcal{J} B$, then any cycling vector w (i) in W[A] is also in W[B].

A second result is also concerned with such a cycling vector w(i). If A is an equivalence class which is minimal with respect to w(i), then for each non-zero component $w_j(i)$ there is a C-signal (α, j) in the corresponding change chart corresponding to a join-irreducible element $\underline{a}$ such that $\underline{a} + w(i)$ is join irreducible and corresponds to $[\alpha + w_j(i), j]$.

This latter result indicates that the set of such changes (α, j) represent a better way of characterizing cyclic behavior of distributive circuits than the equivalence sets which were used with semi-modular circuits.

PART III

MATHEMATICAL METHODS

1. Determination of Interval Size in Numerical Integration of Differential Equations (Supported in part by the National Science Foundation under Grant G2794.)

A method is being sought for automatically determining the interval to be used for numerically integrating a system of ordinary differential equations by the Runge-Kutta method. The requirement is that the solution should have a specified accuracy, and from this specification the interval size is to be adjusted automatically so that it is never smaller than necessary. Professor A. T. Nordsieck of the Physics Department is investigating a method for achieving this result different from that described below.

If the quantities $\bar{y}_i$ are the values given by the Runge-Kutta method for the solution of the differential equation

$$\frac{dy}{dx} = f(x,y)$$

at the points $x_i = x_o + ih$ where i is an integer,

then $y(x_i) = \bar{y}_i + h^5 T_i$ where T_i is the truncation error due to the approximate integration.

We define $\bar{Z}^h_{i+1} = \bar{y}_{i-1} + \frac{h}{3}[f(x_{i-1}, \bar{y}_{i-1}) + 4f(x_i, \bar{y}_i) + f(x_{i+1}, \bar{y}_{i+1})]$

and $\bar{Z}^{2h}_{i+1} = \bar{y}_{i-3} + \frac{2h}{3}[f(x_{i-3}, \bar{y}_{i-3}) + 4f(x_{i-1}, \bar{y}_{i-1}) + f(x_{i+1}, \bar{y}_{i+1})]$

If the $\bar{y}$'s appearing on the right-hand side were replaced by $\bar{Z}$'s, we would have the equations defining the Simpson's rule approximation for the solution of the

differential equation and it would be true that

$$\bar{Z}_i^h = y(x_i) - \frac{h^5}{90} y^{(\bar{v})}(\xi) \qquad x_{i-1} < \xi < x_{i+1}$$

$$\bar{Z}_i^{2h} = y(x_i) \frac{-32h^5}{90} y^{(\bar{v})}(\eta) \qquad x_{i-3} < \eta \leq x_{i+1}$$

These equations hold only approximately in view of the definitions of the $\bar{Z}_i^h$ and $\bar{Z}_i^h$ and $\bar{Z}_i^{2h}$. Nevertheless, it may be shown that a difference equation for the quantities $E_i = \bar{y}_i - y(x_i)$ may be obtained which involves the numbers $A_i = \frac{1}{31}[32(\bar{Z}_i^h - \bar{y}_i) - (\bar{Z}_i^{2h} - \bar{y}_i)]$. This difference equation is being studied with the following question in mind. How must the A_i's and h be restricted so that E_n, the total error after n steps of Runge-Kutta integration is less than a prescribed amount?

2. Monte Carlo Method for Studying Crystals

A program, known as Monte Crysto, to compute the ordering statistics for a binary alloy with face-centered cubic structure and composition A_3B was written last summer for an IBM 704 computing machine. This work is an extension of work done earlier on the ILLIAC where the ordering statistics of a two-dimensional Ising lattice were computed by a Monte Carlo scheme. Results of this early work were reported last spring at the Washington meeting of the American Physical Society and also at the meeting of the Association for Computing Machinery in Houston, Texas. The computational method employed in this work follows very closely that of Metropolis and others in the equation of state calculations for a gas [N. Metropolis, A. Rosenbluth, M. Rosenbluth, A. Teller,

E. Teller, J. Chem. Phys. 21, 1087 (1953)]. Briefly, the Monte Carlo game is arranged to generate a set of configurations which will in the limit, as more and more configurations are generated, produce an ensemble distributed according to Boltzmann statistics [i.e., the probability $p(E_i)$ of generating a configuration, i, with energy E_i at temperature T is proportional to $e^{-E_i/kT}$]. Once the ensemble is generated, the desired physical properties may be obtained by averaging over the members of the ensemble. The Monte Crysto program permits as input parameters: (a) the dimensions of the lattice--maximum is 15 unit cells (4 atoms per cell) on a side; (b) $\frac{v}{kT}$, the ratio of next-neighbor interaction energy to temperature; (c) λ, the ratio of second-neighbor interaction energy to next-neighbor interaction energy. Monte Crysto will compute averages of: (a) the long-range order; (b) The next-neighbor order parameter; (c) the second-neighbor order parameter; (d) standard deviations of these three quantities. Convergence to the Boltzmann distribution is assumed to occur when results from a lattice with an initial configuration of perfect order "agree" with those from a lattice with an initially random configuration. Monte Crysto calculations have continued this semester by remote control on the 704's located at Argonne and MURA.

Recent calculations with the Monte Crysto program have produced good results for the order parameters at temperatures above the order-disorder transition temperature (the Curie temperature, above which long-range order vanishes). However, at lower temperatures convergence of the Monte Carlo process has not been achieved. The reason for this appears to be due to the inability of the lattice, initially started with a random configuration, to establish a consistent pattern of order-- the tendency being to establish only

small regions of local order but almost no long-range order. Alternate schemes for accelerating the convergence by partial ordering were tried but seemed unsuccessful. This consisted of establishing a small, perfectly ordered, region in the lattice with the initially random configuration to serve as a nucleus for the growth of a pattern of order. Different sizes for the ordered region were tried without success.

3. Logical Programming (Supported in part by the Office of Naval Research under Contract N6ori-07130)

A study in programming has been undertaken in which a program will be written for testing equivalence of a pair of given programs. Thus, program A will be used to determine whether given programs B and C perform the same transformation upon given data. It is hoped that program A may then be used to perform transformations upon a program A^1 which is identical to A. The former use of program A may be regarded as equivalent to the execution of mathematical proofs concerning the system described by B and C, and the latter use as equivalent to the execution of metamathematical proofs which may affect the handling of systems B and C.

In order to carry out this study, it is helpful to use a system of machine instructions which admits a simple description. The tentative system chosen consists of two four-address instructions: one for sensing individual binary digits in the memory, and one for altering the memory contents. Program A, referred to above, tests equivalence by breaking down any program into a canonical form which is unique for a given transformation upon a set of data. Such canonical forms are then compared directly.

PART IV

GENERAL RESEARCH

Satellite Data Reduction

A final program to analyze the satellite interferometer data was prepared and placed in production. The method of machine minimization developed by Dr. D. B. Gillies was incorporated in the program. This was concluded to be close to optimum within the limitations imposed by running time, memory space and register length. It is contemplated that this investigation should lead to a library program and possibly to a survey-type paper.

PART V

ILLIAC USE AND OPERATION - GENERAL LABORATORY INFORMATION

Machine Use

During December specifications were presented for 6 new problems. This list does not indicate how the Illiac was used because large amounts of machine time may have been consumed by problems with numbers less than 1084.

1084 Psychology. Attenuation in Factor Analysis. This is a preliminary investigation into the effects of attenuated tests on the obtained factor loadings.

1085 V. A. Research Hospital (Psychiatry). The Relationship Between Psychiatric Diagnostic Information and Therapist Conceptualization of the Patient. The aim of the study is to evaluate the relative utility of the various types of psychiatric diagnostic information for the therapists conceptualization of the psychiatric patient. The study will attempt to discover how, in what ways, and to what extent standard psychiatric and psychological information is utilized by therapists in altering their original views of patients. A Q sort instrument was administered to 18 psychiatrists three times under varying amounts and kinds of information. Three separate correlational matrices (18 x 18) are needed, one for each experimental condition. Three independent factor analyses and rotational solutions will then be carried out--the aim being in each case to determine the dimensions of therapists conceptualization under each condition.

1086 Physics. Superconducting Phase Transition. In order to calculate an energy gap in the theory of superconductivity from the phase diagram, one must know the relation between the critical field H_c and temperature T very accurately. Measurements have been completed of these values which are accurate enough to differentiate and obtain an energy gap. It is proposed to fit these data to the expansion

$$H_c = H_o + \sum_{n=2}^{n} a_n T^n$$

by a least squares method.

1087 Computer. Flow-Gating Flipflop Analysis. This program analyzes the output voltages and currents to establish the holding conditions, saturation conditions, etc., for the "flow-gating" type flipflop given nominal values of the resistors, power supply voltages, transistor parameters, diode parameters and their tolerance limits.

1088 Electrical Engineering. Crystal Lattice Filter Design. For a given set of design requirements, such as the cut-off frequencies of the pass band, the frequencies of infinite attenuation, and the characteristic impedance of the filter, the parameters of the filter are computed. The equations for this wide band, crystal lattice filter were developed by Dr. W. P. Mason, of Bell Telephone Laboratories, and require repeated calculations to obtain a suitable design.

1089 Electrical Engineering. High Pass Filter Design. The problem involves calculation of transfer loss of a filter network with variation in cut-off and resonant frequencies as well as coil Q's and number of sections.

Table I shows the distribution of machine time for the month of December.

Table I

	Hrs:Min
Regular Maintenance	36:00
Unscheduled Maintenance	2:15
Drum Engineering	40:34
R.A.R.	4:47
Leapfrog	33:37
Wasted	:03
Use by Departments	
Computer	74:42
Physics	21:50
Control Systems Lab.	75:44
Struct. Res.	57:09
Struct. Res. (AF 24994)	9:45
Psychology	21:11
Psychology (PH M1733)	4:29
College of Medicine	7:12
Electrical Engineering	11:18
Chemistry	21:43
Agriculture	11:55
Theor. and Appl. Mech. (ORD 593 IC)	:06
Theor. and Appl. Mech. (CONVAIR)	1:20
State Water Survey	7:39
Inst. of Communications Research	6:45
U. S. Navy	1:04
Veteran's Administration (Psychiatry)	:54
Classes	21:26
Demonstrations	:57
Miscellaneous	16:08
	490:33

Error Frequency and Analysis

The machine is normally used for "engineering" and maintenance between 7:00 A.M. and 11:00 A.M., and for a check of its performance between 5:30 and 6:00 P.M. of each weekday. Since the periods between 7:00 and 11:00 A.M., together with certain irregular periods like Saturdays and Sundays, are devoted to a heterogeneous group of functions, it is more instructive from an error standpoint to look at the periods between 11:00 A.M. and 7:00 A.M. of the next day in order to make an observation of the error frequency in the machine. This is the actual period when the machine is designated for use. With this in mind, a summary table has been prepared using the period between 11:00 A.M. and 7:00 A.M. of the next day. This table lists the running time when the machine was operating, the amount of time devoted to repairs because of breakdowns, and a number of failures while the machine was listed as running. During the 5:30-6:30 period (when the machine is checked) if no errors are found, the time is given to the "running" column. Each failure was considered to have terminated a running period and was followed by a repair period in preparing this table. Since the leapfrog code is our most significant machine test, the length of time which it has been used on the machine is listed separately together with the number of errors associated with that particular code. This information for the month is presented in Table II.

It is important to notice that any interruption of machine time that was not planned for is considered a failure in this table. In rare cases where the failure is not known until a later time, it is possible that no repair period is associated with the failure. This over-all system has been adopted because it makes it possible for a machine user to estimate directly the

probability that the machine will be "running" at any instant of time and the probability of a failure during any given interval of running time.

Table III presents a summary of errors or interruptions for December.

TABLE III

Punch Errors	8
Arithmetic Error	1
Drum Errors	4
Unknown Errors	3
	16

TABLE II

DATE	RUNNING OK TIME	REPAIR TIME	INTERRUPTIONS OR FAILURES STOPPING OK TIME	TYPES OF INTERRUPTIONS OR FAILURES CAUSING REPAIR TIME	WASTED	LEAPFROG	FAILURES STOPPING LEAPFROG
12/2/57	19:58	:02	2	(1) Punch No. 4 error extra 2 hole (2) Punch No. 4 error extra 2 hole	:00	:40	0
12/3/57	19:40	:20	2	(1) Punch No. 4 not punching 1 hole (2) Drum failure	:00	:39	0
12/4/57	19:58	:02	1	(1) Punch No. 3 error	:00	:42	0
12/5/57	20:00	:00	0		:00	:41	0
12/6/57	19:34	:26	2	(1) Unknown (2) Unknown	:00	:39	0
12/9/57	20:00	:00	0		:00	:42	0
12/10/57	20:00	:00	0		:00	:51	0
12/11/57	20:00	:00	0		:00	:44	0
12/12/57	19:06	:45	1	(1) Arithmetic error	:00	1:20	0
12/13/57	19:43	:17	1	(1) Drum failure	:00	:40	0
12/16/57	20:00	:00	0		:00	1:16	0
12/17/57	19:59	:01	1	(1) Punch No. 1 failed to punch "8" hole	:00	:39	0
12/18/57	19:59	:01	1	(1) Punch No. 1 failed to punch "4" hole	:00	1:01	0
12/19/57	19:25	:35	2	(1) Drum failure (2) Punch No. 3 jammed	:03	2:08	0
12/20/57	20:00	:00	0		:00	:51	0
12/23/57*	16:00	:01	1	(1) Possibly a line failure at 4:01 A.M. caused trouble	:00	:40	0
12/26/57	20:00	:00	0		:00	:40	0
12/27/57	20:00	:00	0		:00	1:08	0
12/30/57	19:11	:12	1	(1) Drum Failure	:00	1:57	0
12/31/57**	7:36	:01	1	(1) Punch No. 4 error	:00	:00	0
TOTALS	380:09	3:26	16		:03	17:58	0

* Computer shut down at 4:01 A.M.
** Computer Shut down at 7:37 P.M.

Reports and Seminars

Seminars

"The Word Arrangement Core Memory Proposed for the New Computer", by K. C. Smith, December 3, 1957.

"Proposed Core Memory II", by Christopher Pottle, December 10, 1957.

"Cryotron Circuits", by Gene Leichner, December 17, 1957.

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